TECHNICAL MANUAL

ORGANIZATIONAL MAINTENANCE MANUAL
DATA COMMUNICATIONS EQUIPMENT MAINTENANCE

ECPANDED TROUBLESHOOTING
(LOGIC DIAGRAM THEORY)

GUIDED MISSILE AIR DEFENSE SYSTEM
AN/TSQ-73

HEADQUARTERS, DEPARTMENT OF THE ARMY

28 OCTOBER 1982

CHANGE }
No. 2 }

HEADQUARTERS
DEPARTMENT OF THE ARMY
Washington, D.C., 22 January 1987

Organizational Maintenance Manual: Communications Equipment Maintenance

Expanded Troubleshooting (Logic Diagram Theory)

GUIDED MISSILE AIR DEFENSE SYSTEM AN/TSQ-73

TM 9-1430-655-20-7-2, 28 October 1982, is changed as follows:

1. Remove old pages and insert new pages as indicated below. New or changed material is indicated by the applicable change number, i.e., Change 2, at the bottom of the page adjacent to the page number. Revised text will have a vertical bar in the margin next to the changed area. Revised illustrations will have a suffix change letter added to the identification number.

Remove Pages	Insert Pages
A/(B blank)	A/(B blank)
5-89/(5-90 blank)	5-89/(5-90 blank)

2. File this change sheet in front of the publication for reference.

By Order of the Secretary of the Army:

JOHN A. WICKHAM, JR.
General, United States Army
Chief of Staff

Official:

R. L. DILWORTH
Brigadier General, United States Army
The Adjutant General

Distribution:

To be distributed in accordance with DA Form 12-32, Organizational Maintenance requirements for AN/TSQ-73 Missile System.

CHANGE }
No. 1

HEADQUARTERS
DEPARTMENT OF THE ARMY
Washington, D.C., *28 May 1986*

Organizational Maintenance Manual: Communications Equipment Maintenance

Expanded Troubleshooting (Logic Diagram Theory)

GUIDED MISSILE AIR DEFENSE SYSTEM AN/TSQ-73

TM 9-1430-655-20-7-2, 28 October 1982, is changed as follows:

1. This change should not be posted until MWO 9-1425-655-50-3 has been accomplished.

2. Remove old pages and insert new pages as indicated below. New or changed material is indicated by the applicable change number, i.e., Change 1, at the bottom of the page adjacent to the page number. Revised text will have a vertical bar in the margin next to the changed area. Revised illustrations will have a suffix change letter added to the identification number.

Remove Pages	Insert Pages
A/(B blank)	A/(B blank)
i and ii	i and ii
5-5 thru 5-8	5-5 thru 5-8
5-69/(5-70 blank)	5-69/(5-70 blank)
5-85 and 5-86	5-85 and 5-86

By Order of the Secretary of the Army:

JOHN A. WICIXHAM, JR.
General, United States Army
Chief of Staff

Official:

R. L. DILWORTH
Brigadier General, United States Army
The Adjutant General

Distribution:
To be distributed in accordance with DA Form 12-32, Organizational Maintenance requirements for the AN/TSQ-73 Missile System.

3. File this change sheet in front of the publication for reference.

WARNING

DANGEROUS VOLTAGE

is used in the operation of this equipment

DEATH ON CONTACT

may result if personnel fail to observe safety precautions

Never work on electronic equipment unless there is another person nearby who is familiar with the operation and hazards of the equipment and who is competent in administering first aid. When the technician is aided by operators, he must warn them about dangerous areas.

Whenever possible, the power supply to the equipment must be shut off before beginning work on the equipment. Take particular care to ground every capacitor likely to hold a dangerous potential. When working inside the equipment, after the power has been turned off, always ground every part before touching it.

Be careful not to contact high-voltage connections when installing or operating this equipment.

Whenever the nature of the operation permits, keep one hand away from the equipment to reduce the hazard of current flowing through vital organs of the body.

WARNING

Do not be misled by the term "low voltage." Potentials as low as 50 volts may cause death under adverse conditions.

EXTREMELY DANGEROUS POTENTIALS

greater than 500 volts exist in the following units:

Display console high voltage power supply

Display console CRT

WARNING

For emergencies requiring immediate shutdown of system power, press SYSTEM POWER OFF switch located on power cabinet power transfer unit. Observe that SYSTEM POWER ON indicator light goes off.

LIST OF EFFECTIVE PAGES

Insert latest change pages, dispose of superseded pages in accordance with applicable regulations.

NOTE: The portion of the text affected by the changes is indicated by a vertical line in the outer margins of the page.

Dates of issue for original and change pages are:

Original ..... 0 ..... 28 Oct 82
Change ..... I ..... 28 May 86
Change ..... 2 ..... 22 Jan 87

Page No	*Change No
a	0
b Blank	0
A	2
B Blank	2
i	1
ii--iv	0
5-1 - 5-3	0
5-4 Blank	0
5-5 - 5-8	1
5-9	0
5-10 Blank	0
5-1 - 5-23	0
5-24 Blank	0
5-25 - 5-27	0
5-28 Blank	0
5-29	0
5-30 Blank	0
5-31	0
5-32 Blank	0
5-33 - 5-35	0
5-36 Blank	0
5-37--5-41	0
5-42 Blank	0
5-43	0
5-44 Blank	0
5-45--5-47	0
5-48 Blank	0
5-49	0
5-50 Blank	0
5-51 -- 5-53	0
5-54 Blank	0
5-55	0
5-56 Blank	0
5-57	0
5-58 Blank	0
5-59	0
5-60 Blank	0
5-61	0
5-62 Blank	0
5-63 - 5-65	0
5-66 Blank	0
5-67	0
5-68 Blank	0
5-69	1
5-70 Blank I	1
5-71	0
5-72 Blank	0
5-73	0
5-74 Blank	0
5-75	0
5-76 Blank	0
5-77 -5-79	0
5-80 Blank	0
5-81 - 5-85	0
5-86	1
5-87 - 5-88	0
5-89	2
5-90 Blank	2

*Zero in this column indicates an original page.

TM 9-1430-655-20-7-2

TECHNICAL MANUAL
NO. 9-1430-655-20-7-2

HEADQUARTERS
DEPARTMENT OF THE ARMY
WASHINGTON, D.C., 28 October 1982

ORGANIZATIONAL MAINTENANCE MANUAL: DATA COMMUNICATIONS EQUIPMENT MAINTENANCE EXPANDED TROUBLESHOOTING (LOGIC DIAGRAM THEORY) GUIDED MISSILE AIR DEFENSE SYSTEM AN/TSQ-73

REPORTING ERRORS AND RECOMMENDING IMPROVEMENTS

You can help improve this publication. If you find any mistakes, or if you know of a way to improve the procedures, please let us know. Mail your letter, DA Form 2028 (Recommended Changes to Publications and Blank Forms), or DA Form 2028-2 located in back of this manual direct to: Commander, U.S. Army Missile Command, ATTN: AMSMI-LC-ME-PMC, Redstone Arsenal, AL 35898-5238. A reply will be furnished to you.

TABLE OF CONTENTS

TABLE OF CONTENTS - Continued

LIST OF ILLUSTRATIONS

LIST OF TABLES

CHAPTER 5

DATA COMMUNICATIONS EXPANDED TROUBLESHOOTING

Section I. INTRODUCTION

5-1. Scope. This manual is part two TM 91430655207, communications equipment organizational maintenance for Guided Missile Air Defense System AN/TSQ73, and provides supplemental expanded troubleshooting information. This manual is published for the use and guidance of advanced personnel responsible for repair of the data communications beyond the scope of organizational maintenance covered in the basic TM 9143065520 series technical manuals.

5-2. Expanded Troubleshooting Concept. Expanded troubleshooting is required when existing fault isolation procedures in the basic manuals fail to isolate and correct a malfunction. The troubleshooting covered in this manual is based on use of existing onsite equipment (tapes, tools, test equipment, spare parts, and publications). Isolation of malfunctions is based on fault analysis of normal system operating conditions and use of built-in M&D software programs.

5-3. Troubleshooting Aids. This manual contains functional logic diagrams to enhance troubleshooting and fault isolation capabilities. The functional logic diagrams and the associated circuit descriptions are intended to be self-contained and minimize requirements for additional troubleshooting aids. Also, power distribution diagrams, cabling diagrams, and front panel schematic diagrams are supplied.

a. *Input/Output Tables*. Input and output tables are provided as applicable for each figure and sheet to enable easy access to signals referenced to other diagrams.

b. *Input and Output Symbology*. Symbols used on diagrams to indicate input and output signals include the following:

Δ Indicates input from another figure.
■ Indicates output to another figure.

c. *Equipment Interface.* The troubleshooting diagrams may reference inputs and outputs interfacing between other equipments. When there is a notation that an external equipment is involved, it is assumed that the user will refer to the applicable troubleshooting information provided for that equipment.

d. *Logic Symbology*. Logic symbology depends on card types. For discrete circuit cards containing conventional integrated circuits, conventional logic symbols are used. These symbols are used independently with card locations and card pin numbers notated with the symbol. For analog circuits, circuit card details are provided only to a functional level.

5-4. Physical Description (fig.5-1). The data communication equipment consists of a data terminal set (DTS) which includes a data communications control panel 1A1A2A2, an upper modem 1A1A2A5, a communications card cage 1AIA2A6, and a lower modem lA1A2A7. DTS communications interface to external subscribers is accomplished through communications patching panel 1A3A40 and the communications demarkation panel.

a. *Data Terminal Set*. The DTS consists of a data communication control panel, three card cage assemblies, modems, an interim battery data link (IBDL) circuit card, a common timing circuit card, and power supplies. The data communication control panel contains all DTS controls and indicators. Two of the three card cages (upper and lower modem) provide card slots for up to 32 modems. Each modem consists of a set of eight circuit cards. Refer to table 51 for card locations of each modem. The third card cage contains the IBDL and common timing circuit cards. All power for the DTS is supplied from the system power cabinet to dc/dc converters. The number of dc/dc converters used depends on the number and location of modems.

b. Communications Patching Panel. The communications patching panel is located on the right side of the voice communications control unit 1A3A41 and is hinged on the right for easy access. The panel provides eight sets of jacks for each modem, with the transmit and receive pair for a specific net side by side. Each of the jacks is a bantam 2+1 set. The top jack permits entry via a patchcord to the addressee. The middle jack permits entry via a patchcord to the internal equipment and the bottom jack permits monitoring, without breaking the connection, between the internal equipment and the external addressee.

c. Communications Demarkation Panel. The communications demarkation panel is located at the back of the voice communications central unit and extends through the electrical equipment shelter wall. The panel contains 39 rfi filters to limit lightning-induced transients up to 10 kv/microsecond. Table 52 provides a cross-reference list of part and drawing numbers for the AN/TSQ-73 system in reference designator order; this cross-reference is for identification of assembly and electrical drawings only. Refer to TM 9-1430-655-20-1 for a listing of wiring harnesses and cables and associated wire list or cable wiring diagrams.

Table 5-1. Upper and Lower Modem Card Locations

Modem no	Modem control	Modem analog	Modulator carrier generator	Modulator data formatter	Frequency discriminator LP filter	Data synchronizer	I/O control no. 2	I/O control no. 1
1, 17	A1 1102	A1103	A1104	A1105	A1106	Al 1107	A1108	A1109
2, 18	A111110	A1111	A1112	A1113	A1114	A1115	A1116	A1117
3, 19	A1118	A1119	A1120	A1121	A1122	A1123	A1124	A1125
4, 20	A1126	A1127	A1128	A1129	A1130	A1131	A1132	A1133
5, 21	A1201	A1202	A1203	A1204	A1205	A1206	A1207	A1208
6,22	A1209	A1210	A1211	A1212	A1213	A1214	A1215	A1216
7, 23	A1217	A1218	A1219	A1220	A1221	A1222	A1223	A1224
8, 24	A1225	A1226	A1227	A1228	A1229	A1230	A1231	A1232
9, 25	A1302	A1303	A1304	A1305	A1306	A1307	A1308	A1309
10, 26	A1310	A1311	A1312	A1313	A1314	A1315	A1316	A1317
11, 27	A1318	A1319	A1320	A1321	A1322	A1323	A1324	A1325
12, 28	A1326	A1327	A1328	A1329	A1330	A1331	A1332	A1333
13, 29	A1401	A1402	A1403	A1404	A1405	A1406	A1407	A1408
14,30	A1409	A1410	A1411	A1412	A1413	A1414	A1415	A1416
15, 31	A1417	A1418	A1419	A1420	A1421	A1422	A1423	A1424
16, 32	A1425	A1426	A1427	A1428	A1429	A1430	A1431	A1432

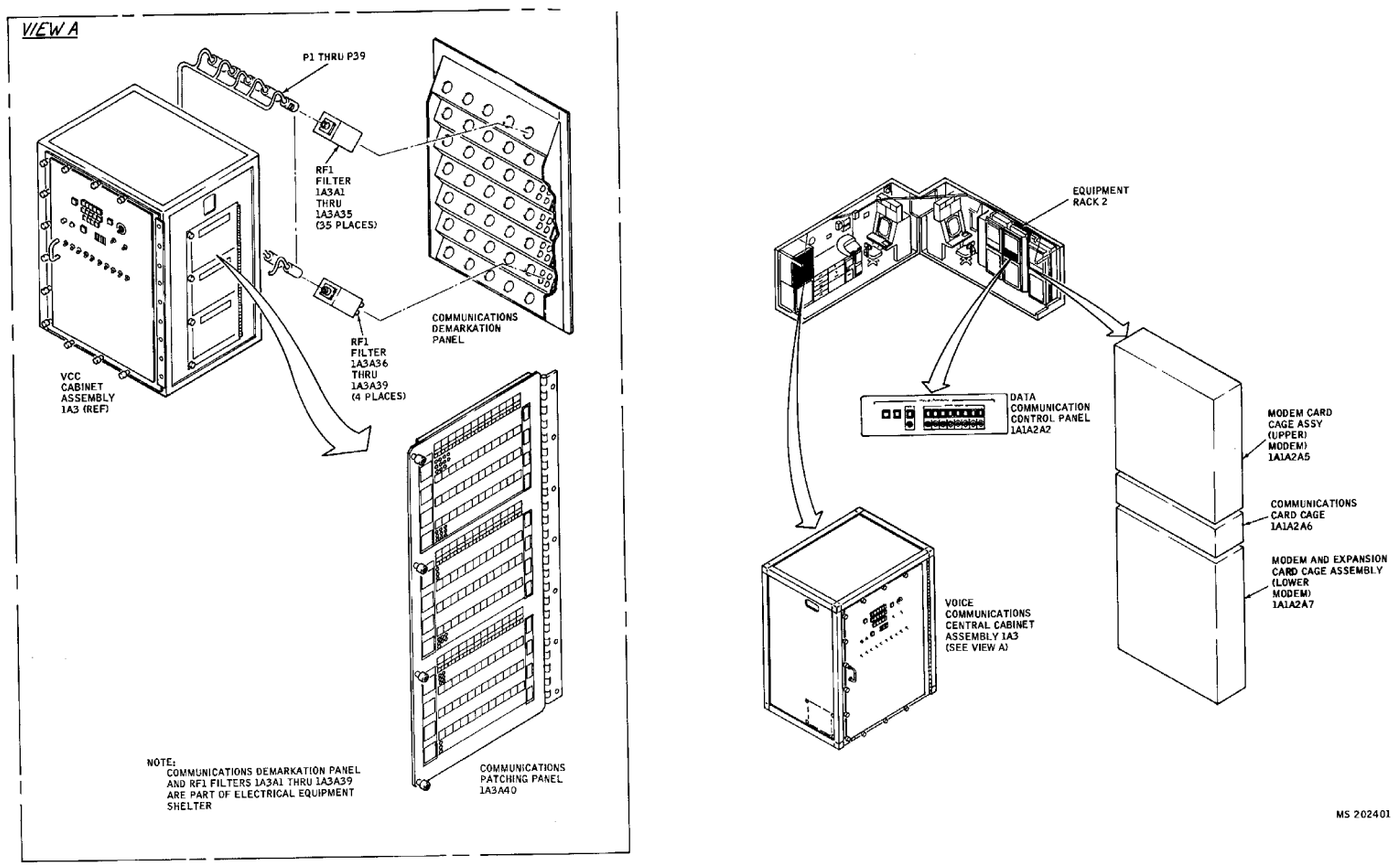


Figure 5-1. Data Communications Equipment, Major Units and Assemblies

5-3/(5-4 blank)

Table 5-2. AN/TSQ-73 Major Equipment Cross-Reference

Ref des	Equipment	Part no	Drawing
--	External Cable Set	10281356	10284717
1	ShelterMultiple	-	
	Intra-Shelter Cable Set	10282262	10284718
1A1	Equipment Rack	10284818	
	Equipment Rack Cable Set	13143776	13143904
1A1A1	Rack 1	-	-
1A1A1A1	RIE II Panel	13143932	WL13143774
1A1A1A2	Radar Simulator Panel	10281406	WL10281406
1A1A1A3	Video Simulator Unit (VSU)	10281390	-
	VSU Wired Card Cage	10281348	WL10281348
1AA1AA4	Radar Integration Unit (RIU)	10281380	-
	RIU Bay I Wired Card Cage	10281387	WL10281387
	RIU Bay 2 Wired Card Cage	10281436	WL10281436
1A1A1A5	Video Processor Unit (VPU)	10281383	-
	VPU Bay I Wired Card Cage	10281388	WL10281388
	VPU Bay 2 Wired Card Cage	10281422	WL10281422
1A1A1A6	Radar/Simulator Unit (R/S)	10281614	-
	R/S Unit Wired Card Cage	10281615	WL10281615
1A1A1A7	1-Port 16K CMOS Memory	13143773	-
	Memory Subassembly	13143807	WL13143808
1A1A1A8	Connector Assembly	13143809	WL13143831
1A1A2	Rack 2-		
1A1A2A1	ADP Status and Control Panel	10284664	WL10284664
1AIA2A2	Data Comm Control Panel	10281439	WL10281439
1A1A2A5	Upper Modem (16/16)	10281616	-
	Upper Modem (10/16)	10284971	-
	Upper Modem Wired Card Cage	10281617	WL10281617
1A1A2A6	Data Comm Card Cage	13143920	-
	Data Comm Wired Card Cage	13143921	WL13143921
1AIA2A7	Lower Modem (4/16)	10281618	-
	Lower Modem (2/16)	10284830	-
	Lower Modem Wired Card Cage	10281650	WL10281650
1A1A3	Rack 3		
1A1A3A1	Input/Output Unit (IOU)	13143770	-
	IOU Wired Card Cage	13143791	WL13143791
1A1A3A2	Buffer Unit	13143771	-

Table 5-2. AN/TSQ-73 Major Equipment Cross-Reference-Continued

Ref des	Equipment	Part no	Drawing
	Buffer Un1t W1red Card Cage	13143792	WL13143792
1A1A3A3	Central Process1ng Un1t (CPU)	13143769	
1A1A3A4	CPU Bay 1 W1red Card Cage	13143789	WL13143789
	CPU Bay 2 W1red Card Cage	13143790	WL13143790
1A1A3A5 thru 1A8thru 1A1A3A8	4-Port 32K CMOS Memory	13143910	-
	Memory Subassembly	13143911	WL13143912
1A1A4	R1E 1 Panel	10281409	WL10281409
1A1A5	Radar 1nterface Panel	10284817	WL10281445
1A1A6	ADP 1nterface Panel	13143917	WL13143917
1A2	Power Cab1net	10285434	WL10285257
1A3	Vo1ce Commun1cat1ons Central (VCC)	10285435	-
1A3A1 thru 1A3A35	RF1 F1lter Assembly	M1S-19560	
1A3A36 thru 1A3A39	RF1 F1lter Assembly	M1S-19561	
1A3A40	Commun1cat1ons Patch1ng Panel	10281341	WL10281331
1A3A41	VCC Un1t	10281355	WL10282276
1A1A41A1	VCC Control Panel	10281623	WL10281889
1A3A41A2	VCC W1red Card Cage	10281334	WL10281334
1A4	Ma1ntenance Bench	13143903	-
1A5, 1A6	D1splay Console	10284960	10282130
1A7, 1A17	Data D1splay Group	10281361	10282122
1A8, 1A13	Magnet1c Tape Un1t	10285127	-
	Tape Transport	10285211	-
	Wired MTU Assembly	10285138	WL10285138
1A9, 1A1OA 10	Voice Commun1cat1ons Stat1on (VSC)	10281399	-
	Wired VCS Un1t	10281625	WL10282287
	VCS Front Panel	10281630	WL10281630
	VCS W1red Card Cage	10282277	WL10282277
1A11	MCPE (when suppl1ed)	10284806	-
1A12	Keyboard Pr1nter Un1t	10281464	-
1A14	Module Test Set (MTS)	10281395	-
	Wired MTS Assembly	10281449	WL10281449
	Test Set Probe Assembly	10285061	WL10281447
1A1S5	Environmental Control Panel	10281477	WL10281477

Table 5-2. AN/TSQ-73 Major Equipment Cross-Reference-Continued

Ref des	Equipment	Part no	Drawing
2	Radar Junction Box	10285092	WL10285092
3	Display Junction Box	10284920	WL10284920
4	Motor Generator Set	10285058	-
5	Diesel Engine Generator	-	-

Section II. OVERALL THEORY

5-5. Overall Functional Description (fig. 52). Data communications equipment consists of a data terminal set (DTS), communications patching panel, and communications demarkation panel. The DTS is the primary functional unit of the data communications equipment and permits the exchange of digital data between the automatic data processing equipment (ADPE) and remote communications facilities. The communications patching panel provides, by way of the communications demarkation panel, the patching, monitoring, and interface capability to external shelter and remote subscribers. The DTS contains 32 modems, which, with the use of multiple bit rates and modulation techniques, properly code and decode all digital data communications to other services, assigned fire units, and adjacent Army systems. The DTS communicates with the ADPE by way of an input/output multiplexer (IOM). The IOM expands the ADPE addressing capability by using input/output expanders (IOE) to accommodate the DTS modems. Each IOE services four modems. In the event of system power failure, the DTS contains IBDL circuitry which provides interrogation signals to the batteries and rebroadcasts the reply messages to all batteries. This circuitry also supplies backup power to the ADPE CMOS memories. Timing for all the modems is derived from a common timing circuit contained in the DTS. The common timing circuit provides four clock frequencies to all modems.

5-6. Logic Theory Presentation. The following paragraphs describe the philosophy and techniques utilized to illustrate and support the data communications logic theory. The primary illustrative materials for the logic theory are the detailed logic diagrams located in Volume 2. These are supplemented by functional block diagrams, timing diagrams and tabular data which are integrated into the logic theory.

a. Data communications is divided into three primary functional and physical entities: the modem, the IBDL mode control, and common timing. The modem is further divided into secondary functional logic groups. For purposes of convenient logic analysis, the secondary functional logic groups (the modulator and demodulator) are further broken down into discrete logic groups to which can be assigned unique logical identities. Each of these final levels of logic groups, which can be referred to as primary functional subassemblies, is represented by a logic diagram which may comprise one or several sheets. Each primary functional subassembly is described under a prime heading and is supported by a functional block diagram. Circuits that perform a sequential and predictable logic function are supported by detailed timing diagrams. For circuits whose functions significantly vary with the content of input data or control signals (data formatter), tabular information is included.

b. The functional block diagrams provide simplified illustrative support for the theoretical discussion, emphasizing functional flow and descriptive signal connotation as opposed to the logic diagrams, which necessarily portray individual signal flow and unique mnemonic connotation. The block diagrams are therefore a tool for understanding the operation of the device and will facilitate application of the logic diagrams when isolating a fault.

c. The block diagrams collect various related functional elements (gates, flipflops, counters, etc.) into functional blocks. These functional blocks are directly related to the broken-line enclosed areas reflected on the associated logic diagrams. In addition, the block diagrams contain the primary input and output mnemonics for each functional block. For the purpose of simplicity, both outputs (flipflops J and K) are only shown when logically critical and bused lines are used where practical to illustrate the flow of related signals. Clock inputs and initialization signals are not shown.

d. The data communications descriptive signal names are usually a direct translation of the particular mnemonic. The modem's mnemonic first letter identifies the upper card cage modems I thru 16 (F) or lower card cage modems 17 thru 32 (G). The second letter identifies the particular modem in each card cage (A thru Q with the O omitted). The IBDL mode mnemonics have an A as the first letter. The modem mnemonics, when interfacing with the data communications patching panel, have the channel address 1 thru 32 as the third and fourth mnemonic character and transmit (T) or receive (R) as the fifth mnemonic character. The modem interface with the IOM is identified by an X as the first mnemonic character, with all of the remaining characters identified as follows:

(1) Second character reflecting IOE 1 thru 7 as A thru G respectively.

(2) Third and fourth character reflecting data parity (OP), data lines (00 thru 07), request lines (RO thru R7), enable (EN), command (CM) and indicator (IN).

5-7. Circuit Card and Key Signal Lookup Tables.
Circuit card and key signal lookup tables provide figure references to functional logic diagrams. These lookup tables permit rapid access for locating circuit areas corresponding to circuit card locations or when signal mnemonics are known.

a. Circuit Card Lookup. Table 5-3 provides circuit card locations for the DTS. The circuit card lookup table provides figure and sheet references to logic diagrams when a circuit card at a particular location is suspect. Since a circuit card may be used for different functional applications, multiple references may be provided for a

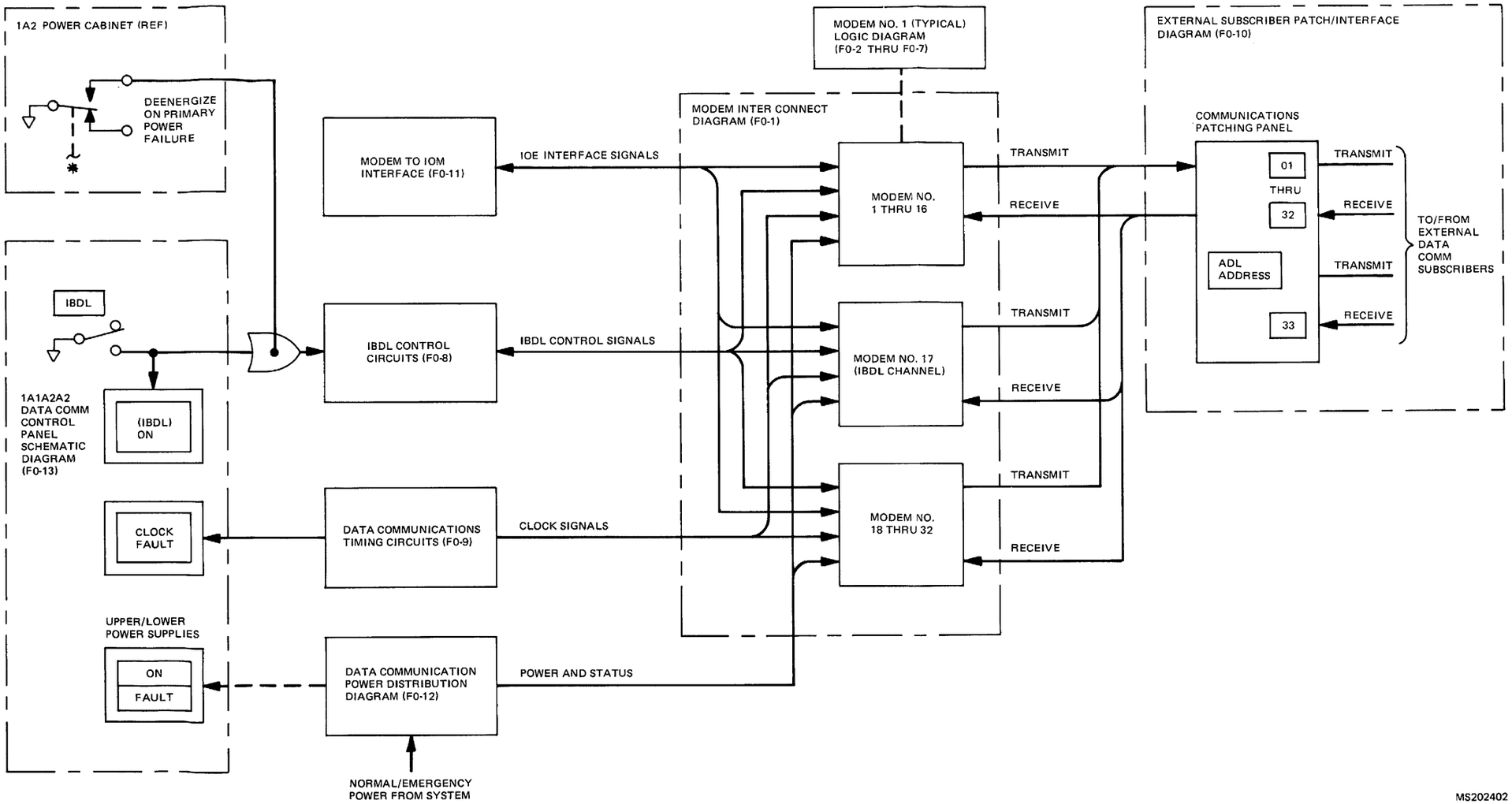


Figure 5-2. Data Communications Block Diagram

single circuit card. The circuit card lookup table also provides information on whether a circuit card is testable by the module test set.

b. *Key Signal Lookup.* Table 54 is a key signal lookup listing for data communications. Key signals are derived by interconnecting signals going between either a physical assembly or a functional circuit area covered by a troubleshooting diagram. Key signals are listed in alphabetical/numerical order (letters precede numbers).

5-8. Modem Interconnect Diagrams (FO1). All modems consist of eight special-purpose circuit cards which are interconnected through the modem card cages. All modems are identical with modem no. 1 except for modem no. 17, which is used for the IBDL mode of operation. The modem complement depends on system configuration; each modem card cage is wired for a full 16modem capacity. Refer to Section III for a detailed description of a modem. Table 51 lists the card locations for each modem.

Table 5-3. Card Location Index

Location	Card slot	Fig.	Sh	Location	Card slot	Fig.	Sh
1A1A2A5	A1101	FO-11	1		A1217	FO-1	7
		FO-9	-		thru		
	A1102	FO-1	1		A1224		
		FO-3	1		A1225	FO-1	8
	A 1103	FO-	11		thru		
		FO-3	2		A1232		
	A1104	FO-1	1		A1301	FO-11	1
		FO-3	1			FO-9	-
		FO-3	2				
		FO-3	2		A1302	FO-1	9
	A1105	FO-1	1		thru		
		FO-2	-		A1309		
	A1106	FG 1	1		A1310	FO-1	10
		FO-4	-		thru		
	A1107	FO-1	1		A1317		
		FO-5	-		A1318	FO-1	11
	A1108	FO- 1	1		thru		
		FO-7	-		A1325		
	A1109	FO-1	1		A1326	FO-1	12
		FO-6	1		thru		
		FO-6	2		A1333		
	A110O	FO-1	2		A1334	FO-9	-
	thru	A1401				FO-1	13
	A 1117				thru		
	A1118	FO-1	3		A1408		
	thru				A1409	FO-1	14
	A1125				thru		
	A1126	FO-1	4		A1416		
	thru				A1417	FO-1	15
	A1133				thru		
	A1134	FO-9	-	1A1A2A5	A1424		
	A1201	FO-1	5	1A1A2A5	A1425	FO-1	16
	thru				thru		
1A1A2A5	A1208				A1432		
1A1A2A5	A1209	FO-1	6	1A2A6	A1124	FO-9	-
	thru						
	A1216			1A1A2A6	A1125	FO-8	1

Table 5-3. Card Location Index-Continued

Location	Card slot	Fig.	Sh	Location	Card slot	Fig.	Sh
1A1A2A7	A101	FG-11 FO-12	2 1-2		A301	FO-11 FO-9	2 -
	A1102 thru A1109	FO-1	17		A1302 thru A1309	FO-1	25
	A1110 thru A1117	FO-1	18		A1310 thru A1317	FO-1	26
	A1118 thru A1125	FO-1	19		A1318 thru A1325	FO-1	27
	A1126 thru A1133	FO-1	20		A1326 thru A1333	FO-1	28
	A1134	FO-9	-		A1334	FO-9	-
	A1201 thru A1208	FO-I	21		A1401 thru A1408	FO-1	29
	A1209 thru A1216	FO-1	22		A1409 thru A1416	FO-1	30
1A1A2A7	A1217 thru A1224	FO-1	23	1A1A2A7	A1225 thru A1424	FO-1	24
1A1A2A7	A1225 thru A1232	FO-1	24	1A1A2A7	A1425 thru A1432	FO-1	32

Table 5-4. Key Signal Lookup

Signal	FO - Sh	Signal	FO - Sh
ATB1YD1	1 - 1 thru 1 - 32, 8-2	ATC15A	1 - 15, 8-2
		ATC16A	1 - 16, 8-2
ATB2YD1	1 - 1 thru 1 - 32, 8 - 2	ATC17A	1 - 17, 8-2
		ATC1OA	1 - 10, 8 -2
ATB3YD1	1-1 thru 1 - 32, 8 - 2	ATC19A	1 - 19, 8-2
		ATC20A	1 - 20, 8 - 2
ATB4YD1	1 - 1 thru 1-32 8 -2, 8-2	3ATC21A	1 - 21, 8 -2
ATCO1A	1 - 1, 8-2	ATC22A	1 - 22, 8-2
ATC02A	1 - 2, 8-2	ATC23A	1 - 23, 8-2
ATC03A	1 - 3, 8-2	ATC24A	1 - 24, 8-2
ATC04A	1 - 4, 8-2	ATC25A	1 - 25, 8-2
ATC05A	1 - 5, 8-2	ATC26A	1 - 26, 8-2
ATC06A	1 - 6, 8-2	ATC27A	1 - 27, 8-2
ATC07A	1 - 7, 8-2	ATC28A	1 - 28, 8-2
ATC08A	1 - 8, 8-2	ATC29A	1 - 29, 8-2
ATC09A	1 - 9, 8 -2	ATC30A	1 - 30, 8-2
ATC 1 OA	1 - 10, 8-2	ATC31A	1 - 31, 8-2
ATC1 1A	1 - 11, 8-2	ATC32A	1 - 32, 8-2
ATC12A	1 - 12, 8 - 2	ATFLTA	9
		ATENDA	1- 17, 8-1
ATC13A	1 - 13, 8-2	ATIBLS	1- 1 thru 1 - 32, 8-2
ATC14A	1 - 14, 8-2		

Table 5-4. Key Signal Lookup-Continued

Signal	FO - Sh	Signal	FO - Sh
ATRETA	1 - 17, 8-1	FF06RA/B	10 - 2, 1-6
ATUSEA	1 - 1 thru 1 - 32	FF06TA/B	10 - 2, 1 - 6
		FG07RA/B	10 - 2, 1-7
ATXENA	1 - 17, 8- 1	FG07TA/B	10 - 2, 1 -8
ATlM5D4	9	FH08RA/B	10 - 2,
AT1M3D4	9		1 - 8
AT15MD4	9	FH08TA/B	10 - 2,
AT48KD4	9		1-8
AT5M2D4	9	FI09RA/B	10 - 3, 1-9
BUSOUT	1 -1 thru 1 - 32, 3 - 2 8-2	FI09TA/B	10- 3, 1-9
		FJIORA/B	10- 3, 1 - 10
DDIPSI-8	1 - 1 thru 12- 32 12 - 1	FJ1OTA/B	10- 3, 1 - 10
		FK11RA/B	10- 3, 1-11
DLSRA/B	10 - 8	FK11TA/B	10 - 3,
DLSTA/B	10 - 8		1 - 11
FAOIRA/B	10- 1, 1-1	FL12RA/B	10 -3, 1 - 12
FAOITA/B	10 - 1, 1-1	FL12TA/B	10 - 3, 1-12
FB02RA/B	10 - 1, 1-2	FM13RA/B	10 - 4, 1 - 13
FB02TA/B	10 - 1, 1-2	FM13TA/B	10 - 4, 1 - 13
FC03RA/B	10 - 1, 1-3	FN14RA/B	10 - 4, 1 - 14
FC03TA/B	10 - 1, 1-3	FN14TA/B	10 - 4, 1 - 14
FD04RA/B	10 - 1, 1-4	FP15RA/B	10 - 4, 1 - 15
FD04TA/B	10 - 1, 1-4	FP15TA/B	10 - 4, 1-15
FE05RA/B	10 - 2, 1-5	FQ16RA/B	10-4 1 -16
FE05TA/B	10 - 2, 1-5	FQ16TA/B	10 - 4, 1 - 16

Table 5-4. Key Signal Lookup-Continued

Signal	FO - Sh	Signal	FO - Sh
FT1M51-8	1 - 1 thru 1 - 32, 9	GC19RA/B	10 - 5, 1 - 19
		GC19TA/B	10 - 5, 1 - 19
FTI5MI-8	1 - 1 thru 1 - 32, 9	GD20RA/B	10- 5, 1 - 20
		GD20TA/B	10- 5, 1 - 20
FT48K1-8	1 - 1 thru 1 - 32, 9	GE21RA/B	10 - 6, 1 - 21
		GE21TA/B	10 - 6, 1 - 21
FT5M21-8	1 - 1 thru 1 - 32, 9	GF22RA/B	10 - 6, 1 - 22
		GF22TA/B	10 - 6, 1 - 22
GABIPA	1 - 17, 8 - 1	GG23RA/B	10 - 6, 1 - 23 8-1
GABIX	1 - 17, 8 - 1	GG23TA/B	10 - 6, 1 - 23 8-1
GAB2X	1 - 17,	GH24RA/B	10- 6, 1 - 24 8-1
GAB3X	1 - 17,	GH24TA/B	10 - 6, 1 - 24 1 - 24
GAB4X	1 - 17, 8-1		
GACYPA	1 - 17,	GI25RA/B	10 - 7, 1 -25
GAFCIA	1 - 17, 8-1	GI25TA/B	10 - 7, 1- 25
GAFCNA	1 - 17, 8-1	GJ26RA/B	10 - 7, 1 -26
GARDYA ‘	1- 17, 8-1	GJ26TA/B	10-7, 1 - 26
GASNPA	1 - 17, 8-1	GK27RA/B	10 - 7, 1 -27
GA17RA/B	10 - 5, 1 -17	GK27TA/B	10 - 7, 1 - 27
GA17TA/B	10 - 5, 1 - 17	GL28RA/B	10 - 7, 1 -28
GB18RA/B	10 - 5, 1 - 18	GL28TA/B	10 - 7, 1 -28
GB18TA/B	10- 5, 1 - 18	GM29RA/B	10 - 8, 1 -29

Table 5-4. Key Signal Lookup-Continued

Signal	FO - Sh	Signal	FO - Sh
GM29TA/B	10 - 8 1 - 29	YD04RA/B	10 - 1
		YD04TA/B	10 - I
GN30RA/B	10 - 8, 1 - 30	YD20RA/B	10- 5
GN30TA/B	10- 8, 1 - 30	YD20TA/B	10- 5
		YE05RA/B	10 - 2
GP31RA/B	10- 8, 1 -31	YEOSTA/B	10- 2
		YE21RA/B	10 - 6
GP31TA/B	10 - 8, 1 - 31	YE21TA/B	10 - 6
GQ32RA/B	10 - 8, 1 - 32	YF06RA/B	10 - 2
		YF06TA/B	10 - 2
GQ32TA/B	10 - 8, 1 - 32	YF22RA/B	10 - 6
		YF22TA/B	10 - 6
GT1M51-8	1 - 17 thru 1 - 32, 9	YF22TA/B YG07RA/B	 10 - 2
		YG07TA/B	10 - 2
		YG23RA/B	10- 6
GT15M1-8	1 - 17 thru 1 - 32, 9	YG23RA/B YG23TA/B	 10 - 6
		YH08RA/B	10 - 2
		YH08TA/B	10 - 2
GT48K1-8	1 - 17 thru 1 - 32, 9	YH24RA/B	10 - 6
		YH24TA/B	10 - 6
		YI09RA/B	10 - 3
GT5M21-8	1 - 17 thru 1 - 32, 9	YI09TA/B	10 - 3
		YI25RA/B	10 - 7
		YI25TA/B	10 - 7
YAO1RA/B	10 - 1	YJ1ORA/B	10 - 3
YAO1TA/B	10 - 1	YJ1OTA/B	10- 3
YA17RA/B	10 - 5	YJ26RA/B	10 - 7
YA17TA/B	10- 5	YJ26TA/B	10 - 7
YB02RA/B	10 - 1	YK11RA/B	10- 3
YB02TA/B	10 - 1	YK11TA/B	10-3
YB18RA/B	10 - 5	YK27RA/B	10 - 7
YB18TA/B	10- 5	YK27TA/B	10-7
YC03RA/B	10 - 1	YL12RA/B	10- 3
YC03TA/B	10 - 1	YL12TA/B	10-3
YC19RA/B	10 - 5	YL28RA/B	10- 7
YC19TA/B	10 - 5	YL28TA/B	10 - 7

Table 5-4. Key Signal Lookup-Continued

Signal	FO - Sh	Signal	FO - Sh
YM13RA/B	10 -4	XAOOAB4	1-1 thru 1-4
YM13TA/B	10-4		
YM29RA/B	10 -8	XAOAB4	1-1 thru 1-4
YM29TA/B	10-8		
YN14TA/B	10-4		
YN30RA/B	10-8		
YN30TA/B	10-8	XAO3AB4	1-1 thru 1-4
YPN30RA/B	10-4		
YP1STA/B	10-4	XAO4AB4	1-1 thru 1-4
YP31RA/B	10-8		
YP31TA/B	10-8	XAO5AB4	1-1 thru 1-4
YQ16RA/B	10-4		
YQ16TA/B	10-4	XA6AB4	1-1 thru 1-4
YQ32RA/B	10-8		
YQ32TA/B	10-8		
YS33RA/B	10-8	PA7AB4	thru 1-4
YS33TA/B	10-8		
XACMSD4	1-1 thru 1-4	XBCMSD4	1-5 thru 1-8
XAENSD4	1-1 thru 1-4	XBENSD4	1-5 thru 1-8
XAINAB4	1-1 thru 1-4	XBINAB4	1-5 thru 1-8
XAROAB4	1-1	XBROAB4	1-5
XAR1AB4	1-1	XBR1AB4	1-5
XAR2AB4	1-2	XBR2AB4	1-6
XAR3AB4	1-2	XBR3AB4	1-6
XAR4AB4	1-3	XBR4AB4	1-7
XAR5AB4	1-3	XBR5AB4	1-7
XAR6AB4	1-4	XBR6AB4	1-8
XAR7AB4	1-4	XBR7AB4	1-8
XAOPAB4	1-1 thru 1 -4	XBOPAB4	1-5 thru 1-8

Table 5-4. Key Signal Lookup-Continued

Signal	FO - Sh	Signal	FO - Sh
XBOOAB4	1-5 thru 1-8	XCOOAB4	1-9 thru 1-12
XBO1AB4	1-5 thru 1-8	XCOlAB4	1-9 thru 1-12
XB02AB4	1-5 thru 1-8	XC02AB4	1-9 thru 1-12
XB03AB4	1-5 thru 1-8	XC03AB4	1-9 thru 1-12
XB04AB4	1-5 thru 1-8	XC04AB4	1-9 thru 1-12
XBO5AB4	1-5 thru 1-8	XCO5AB4	1-9 thru 1-12
XB06AB4	1-5 thru 1-8	XC06AB4	1-9 thru 1-12
XB07AB4	1-5 thru 1-8	XC07AB4	1-9 thru 1-12
XCCMSD4	1-9 thru 1-12	XDCMSD4	1-13 thru 1-16
XCENSD4	1-9 thru 1-12	XDENSD4	1-13 thru 1-16
XCINAB4	1-9 thru 1-12	XDINAB4	1-13 thru 1-16
XCROAB4	1-9	XDROAB4	1-13
XCR1AB4	1-9	XDR1AB4	1-13
XCR2AB4	1-10	XDR2AB4	1-14
XCR3AB4	1-10	XDR3AB4	1-14
XCR4AB4	1-11	XDR4AB4	1-15
XCR5AB4	1-11	XDR5AB4	1-15
XCR6AB4	1-12	XDR6AB4	1-16
XCR7AB4	1-12	XDR7AB4	1-16
XCOPAB4	1-9 thru 1-12	XDOPAB4	1-13 thru 1-16

Table 5-4. Key Signal Lookup-Continued

Signal	FO - Sh	Signal	FO - Sh
XDOOAB4	1-13 thru I-16	XEOOAB4	1-17 thru 1-20
XDO1AB4	1-13 thru 1-16	XEO1AB4	1-17 thru 1-20
XDO2AB4	1-13 thru 1-16	XEO2AB4	1-17 thru 1-20
XD03AB4	1-13 thru 1-16	XEO3AB4	1-17 thru 1-20
XDO4AB4	1-13 thru 1-16	XEO4AB4	1-17 thru 1-20
XDO5AB4	1-13 thru 1-16	XE05AB4	1-17 thru 1-20
XDO6AB4	1-13 thru 1-16	XEO6AB4	1-17 thru 1-20
XD07AB4	1-13 thru 1-16	XEO7AB4	1-17 thru 1-20
XECMSD4	1-17 thru 1-20	XFCMSD4	1-21 thru 1-24
XEENSD4	1-17 thru 1-20	XFENSD4	1-21 thru 1-24
XEINAB4	1-17 thu 1-20	XFINAB4	1-21 thru 1-24
XEROAB4	1-17	XFROAB4	1-21
XERlAB4	1-17	XFRIAB4	1-21
XER2AB4	1-18	XFR2AB4	1-22
XER3AB4	1-18	XFR3AB4	1-22
XER4AB4	1-19	XFR4AB4	1-23
XER5AB4	1-19	XFR5AB4	1-23
XER6AB4	1-20	XFR6AB4	1-24
XER7AB4	1-20	XFR7AB4	1-24
XEOPAB4	1-17 thru 1-20	XFOPAB4	1-21 thru 1- 24

Table 5-4. Key Signal Lookup-Continued

Signal	FO - Sh	Signal	FO - Sh
XFOOAB4	1-21 thru 1-24	XGOOAB4	1-25 thru 1-28
XFO1AB4	1-21 thru 1-24	XGO1AB4	1-25 thru 1-28
XFO2AB4	1-21 thru 1-24	XGO2AB4	1-25 thru 1-28
XFO3AB4	1-21 thru 1-24	XGO3AB4	1-25 thru 1-28
XFO4AB4	1-21 thru 1-24	XGO4AB4	1-25 thru 1-28
XFOSAB4	1-21 thru 1-24	XG05AB4	1-25 thru 1-28
XFO6AB4	1-21 thru 1-24	XGO6AB4	1-25 thru 1-28
XFO7AB4	1-21 thru 1-24	XGO7AB4	1-25 thru 1-28
XGCMSD4	1-25 thru 1-28	XHCMSD4	1-29 thru 1-32
XGENSD4	1-25 thru 1-28	XHENSD4	1-29 thru 1-32
XGINAB4	1-25 thru 1-28	XHINAB4	1-29 thru 1- 32
XGROAB4	1-25	XHROAB4	1-29
XGR1AB4	1-25	XHR1AB4	1-29
XGR2AB4	1-26	XHR2AB4	1-30
XGR3AB4	1-26	XHR3AB4	1-30
XGR4AB4	1-27	XHR4AB4	1-31
XGR5AB4	1-27	XHRSAB4	1-31
XGR6AB4	1-28	XHR6AB4	1-32
XGR7AB4	1-28	XHR7AB4	1-32
XGOPAB4	1-25 thru 1-28	XHOPAB4	1-29 thru 1-32

Table 5-4. Key Signal Lookup-Continued

Signal	FO - Sh	Signal	FO - Sh
XHOOAB4	1-29 thru 1-32	+5PUPI	1-1 thru 1-4, 1-17
XHO1AB4	1-29 thru 1-32		thru 1-20 12-2
XHO2AB4	1-29 thru 1- 32	+5PUP2	1-5 thru 1-8, 1-21 thru
XH03AB4	1-29 thru 1-32		1-24 1-2
		+ 5PUP3	1-9
XH04AB4	1-29 thru 1-32 thru		thru 1-12, 1-25
XH05AB4	1-29 1-32 1-3		1-28
		+5PUP4	1-13
XH06AB4	1-29 thru 1- 32		thru 1-16, 1-29
XH07AB4	1-29 thru 1-32		thru 1-32, 12-2

Section III. MODEM

5-9. General (fig. 53). All 32 modems are functionally identical, with the exception of modem no. 17, which is used for the Interim Battery Data Link (IBDL) mode. The following description is provided for a typical modem, which consists of the following five sections:

Modulator
Demodulator Modem analog
Input/output control no. 1
Input/output control no. 2

The modem accommodates four bit rates, two modulation techniques, seven modulation frequencies, and four message formats. All bit rates and message formats are selected by front panel controls.

a. The required message formats consist of four types:
Missile Battery Data Link (MBDL), Intra Army/Tactical Data Information Link B (IA/TADILB), North Atlantic Treaty Organization (NATO), and a spare link. Table 55 defines the modem parameters for each format selected. The interrogation signal is used only for the MBDL format and is sent to the battery data links at the beginning of each transmission cycle. The synchronization pattern is used to ensure that the timing sequence of the sending station is the same as that of the receiving station. The data that follows the synchronization is broken into data groups, along with a check group that contains parity bits to check the integrity of data transmission between the IOM and the modem.

b. The bit rate is the speed at which the modem transmits and receives information. Refer to table 56 for bit rates and the corresponding modulated frequencies. The bit rates selected at each modem must be the same for the sending and receiving station.

c. The modulation technique is frequency shift keying (FSK) or differential frequency shift keying (DFSK). When the modulation is FSK, the logic zero represents the higher of the two frequencies. The higher frequency is space frequency. The logic one represents the lower of two frequencies and is mark frequency. When the modulation is DFSK, the data group will always begin with a mark frequency. The logic one always represents a change in the frequency, whereas the logic zero will not cause a frequency change.

d. The modem uses an idle signal continuously after the initialization of a link. When the IOM is not providing information to the modem, the modem output is an idle signal. The idle signal is dependent upon the format selected.

(1) *Modulator.* The modulator accepts the 8-bit data byte and device commands from input/output no. 1 and generates an FSK or a DFSK carrier according to the bit rate and format selected. The data formatter provides the functions of command decoding, remote and ready start generation, data byte timing, parallel to serial data conversion, and FSK or DFSK conversion. The data formatter supplies three frequency control inputs, center, mark, and space (Fc, Fm, and Fs), to the carrier generator, and a data strobe to input/output control no. 2. The data strobe allows a transmit request to be generated. The carrier generator converts the frequency control inputs from the data formatter into a 4bit binary signal. The 4bit signal is a binary weighted representation of the audio frequency. The 4bit binary signal is converted to sinusoidal FSK/DFSK output signals by the modem analog.

(2) *Demodulator*. The demodulator converts the FSK/DFSK input signals to binary levels, recognizes message start preambles, performs receive timing synchronization, and controls data and information exchange with input/output interface logic. The modem analog converts the FSK/DFSK input signals to logic level square waves and supplies the limiter carrier to the frequency discriminator/low pass filter. The frequency discriminator converts the half cycle between the high and low carrier into 16 binary levels. The 16 binary levels are converted back to binary data signals by the low pass filter and supplied as low pass filter data to the data synchronizer. The data synchronizer provides the bit rate timing synchronization, start-of-message detection, and serial-to-parallel data conversion.

(3) Modem analog. The modem analog provides digital-to-analog conversion and filtering for the modulator, and bandpass filtering and limiting for the demodulator.

(4) Input/output control no. I. Input/output control no. 1 provides the parallel dc interface necessary to receive data and commands from the IOM. All transfer to and from the IOM is dc-coupled with nominal pulse widths of 180 nanoseconds.

(5) Input/output control no. 2. Input/output control no. 2 provides the dc interface necessary to communicate with the IOM for command acknowledgements, transmit/receive generation, data strobe and controls, EOB detection for the demodulator, preset initialization, and data input.

5-10. Modulator Detailed Description (fig. 54). The modulator consists of a data formatter, a carrier generator, a transmit clock generator, and a portion of the modem analog, which is described in paragraph 512. The modulator can operate at 600, 750, 1200, and 1500 bit rates, and with any one of MBDL, IA/TB, spare, or NATO message formats. The ADP assembles the messages in accordance with the requirements of each

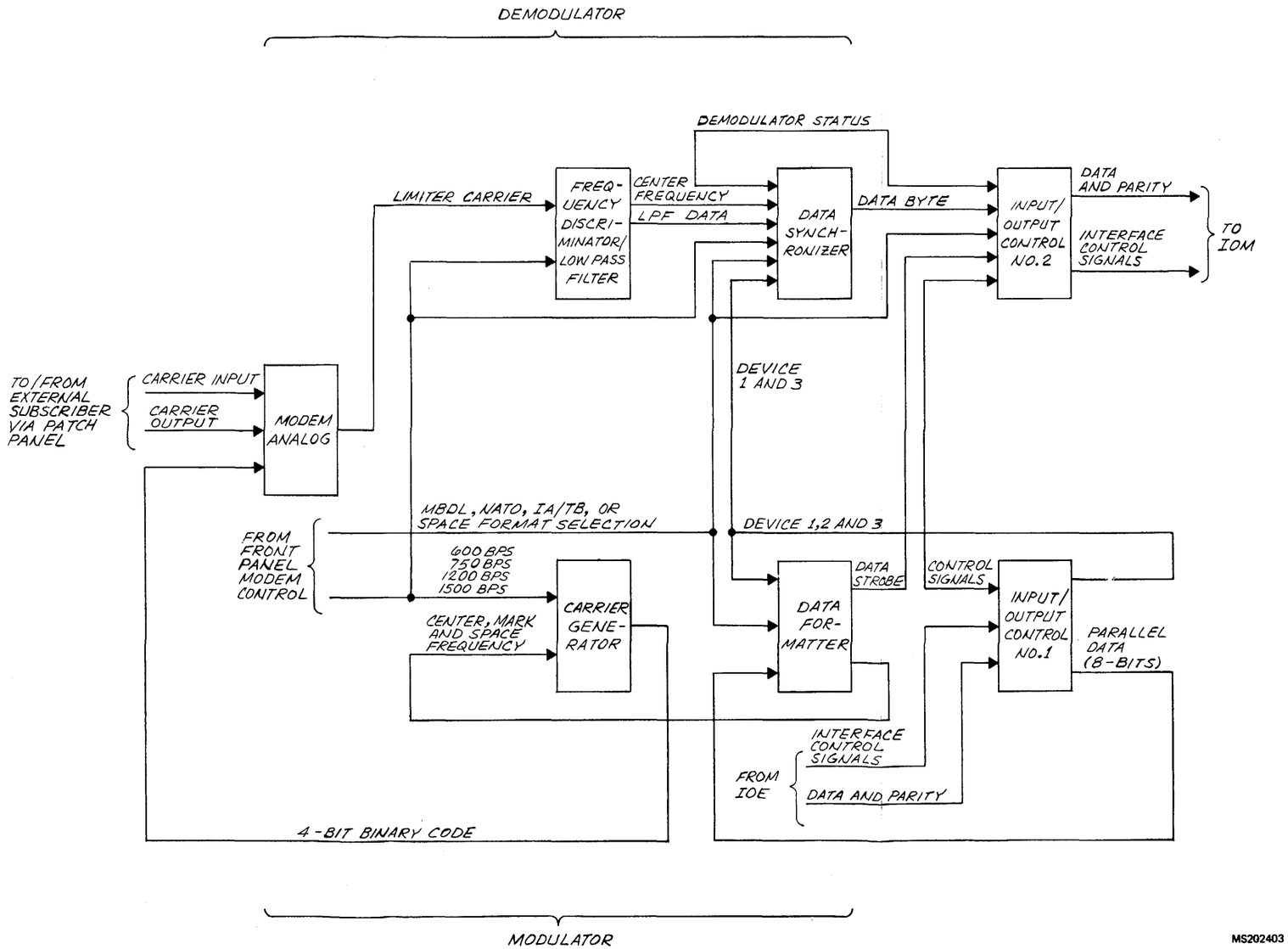


Figure 5-3. Typical Modem Block Diagram

Table 5-5. Message Formats

Parameter	Missile Battery Data Link (MBDL)	Intra-Army/TADIL-B (IA/TB)	Spare format	NATO
Interrogation Signal (Hardware generated)	Remote Start 4 bits f_C 4 bits f_s	N/A	N/A	N/A
Total Bits per Message (Software generated)	59	72 (TADIL-B) 81 (Intra-Army)	72/128	64/120/128
Synchronization Pattern (Hardware generated)	9 bits 4 bits f_c 3 bits f_m 1 bit f_s 1 bit f_m	9 bits All f_s	8 bits All f_c	8 bits of Logic zero
Data Group (Software generated) bits	50 bits incl 1 parity and 1 guard bit	Six or nine 9-bit groups of 1 mark bit and 8 data bits bit and 7 data	7 or 14 8-bit groups of 1 mark bit and 7 data bits	6, 13, or 14 8-bit groups of 1 mark
Check Group (Software generated)	1 parity bit 8 parity bits parity bits	9-bit group of 1 mark bit and mark bit and 7 parity bits	8-bit group of 1 mark bit and 7	8-bit group of 1
Bit Rate (BPS) 1500)	750 (600, 1200, 1500)	600/1200 (750, 1500) 1500)	600/1200 (750,	600/1200 (750,
Modulation	FSK	FSK	FSK	DFSK
Technique				
Logic one	f_m = low freq	f_m= low freq	f_m = low freq	Change in freq
Logic zero (Hardware generated)	f_s = high freq frequency	f_s= high freq	f_s = high freq	No change in
Idle Signal (Hardware generated)	Logic zero (f_s) (f_m/f_s)	Alternating 1/0 ($f_m/f_{s)}$	Alternating 1/0 ($f_m/f_{s)}$	Logic 1

LEGEND: f_m = mark frequency
f_s = space frequency
f_c = center frequency
N/A = not applicable

NOTE: Bit rates shown without parentheses are standard.

Table 5-6. Bit Rates and Modulation Frequencies

	Modulation frequencies		
Bit rate (BPS) Bits per second	$f_{m\ (hz)}$	$f_{c\ (Hz)}$	$f_{s\ (Hz)}$
600	1300	1500	1700
750	1125	1500	1875
1200	1300	1700	2100
1500	1125	1875	2625

NOTE: f_m = mark frequency for FSK links
fc= center frequency
f_s = space frequency for FSK links

interface (fire unit, adjacent battalions, remote radars, etc.) and supplies the messages to the modulator. The modulator accepts the command instructions and parallel data bytes from input/output control no. 1 and generates an FSK or a DFSK carrier, as required. The device control commands are the device I and the device 2 or 3. If the device command is a device 1 and the MBDL message format is selected, the modulator will respond by transmitting an interrogation (remote start) message and then a ready start before requesting and transmitting data bytes. If the device command is a device 2 or device 3, the modulation transmits a ready start and requests and transmits the data bytes. The data formatter accepts the device control command and data inputs and converts the inputs into three frequency control outputs (center, mark, and space frequency) and data strobe. The three frequency control outputs are obtained by parallel-to- serial conversion of the data inputs, which are then supplied to an FSK or a DFSK converter. The transmit bit rate clock from the transmit clock generator provides the output frequency rate for the three frequencies in accordance with the bit rate selected. The data strobe from the data formatter allows a transmit request to be generated to the IOM. A transmit request is generated with each data strobe until a transmit EOB is recognized from the IOM. The transmit EOB causes the modulator to cease requesting data. The carrier generator accepts the parallel-to-serial data represented by the three frequency outputs and converts the input data into a 4-bit binary code which is the output carrier signal. The 4-bit binary code is reflected as a modified staircase waveform. The modem analog then converts the 4-bit binary code to sinusoidal FSK/DFSK output signals. During the IBDL backup mode, a dedicated modem (no. 17) is used and operates in only the MBDL format. The bit clock from the data synchronizer and the IBDL remote and transmit signals are applicable to the IBDL mode of operation. Refer to section IV for IBDL mode description.

a. *Data Formatter* (fig. 5-5, FO-2). The data formatter generates the center, mark, and space frequency indications required by the carrier generator during the transmit mode. The data formatter operation is initiated by the device command from the input/output control. The actual frequency pattern generated is dependent upon the mode currently selected. The data formatter is capable of operating in the MBDL, TADIL-B, INTRA-ARMY, or NATO format. Since most of the logic is utilized during the MBDL mode but is common to all modes, it will be assumed that the MBDL mode is selected, a device 1 command is received, a transmit address is active, and a repetitive byte pattern of 11000110 is to be transmitted. A timing diagram of the data formattter operation is illustrated in figure 5-6.

(1) The data formatter provides four modes of operation: idle, remote start, ready start, and data modes. The idle mode for MBDL is defined as all space frequency. Upon receiving the device 1 command, the command is stored in the command register. After storing the command, the data formatter transmits a remote start and ready start message followed by data bytes. Once in the data mode, the data formatter remains in that mode until EOB is sensed and the device command is terminated. At this time, the data formatter returns to the idle mode. Table 5-7 lists the frequency control and data strobe outputs during the four modes of operation.

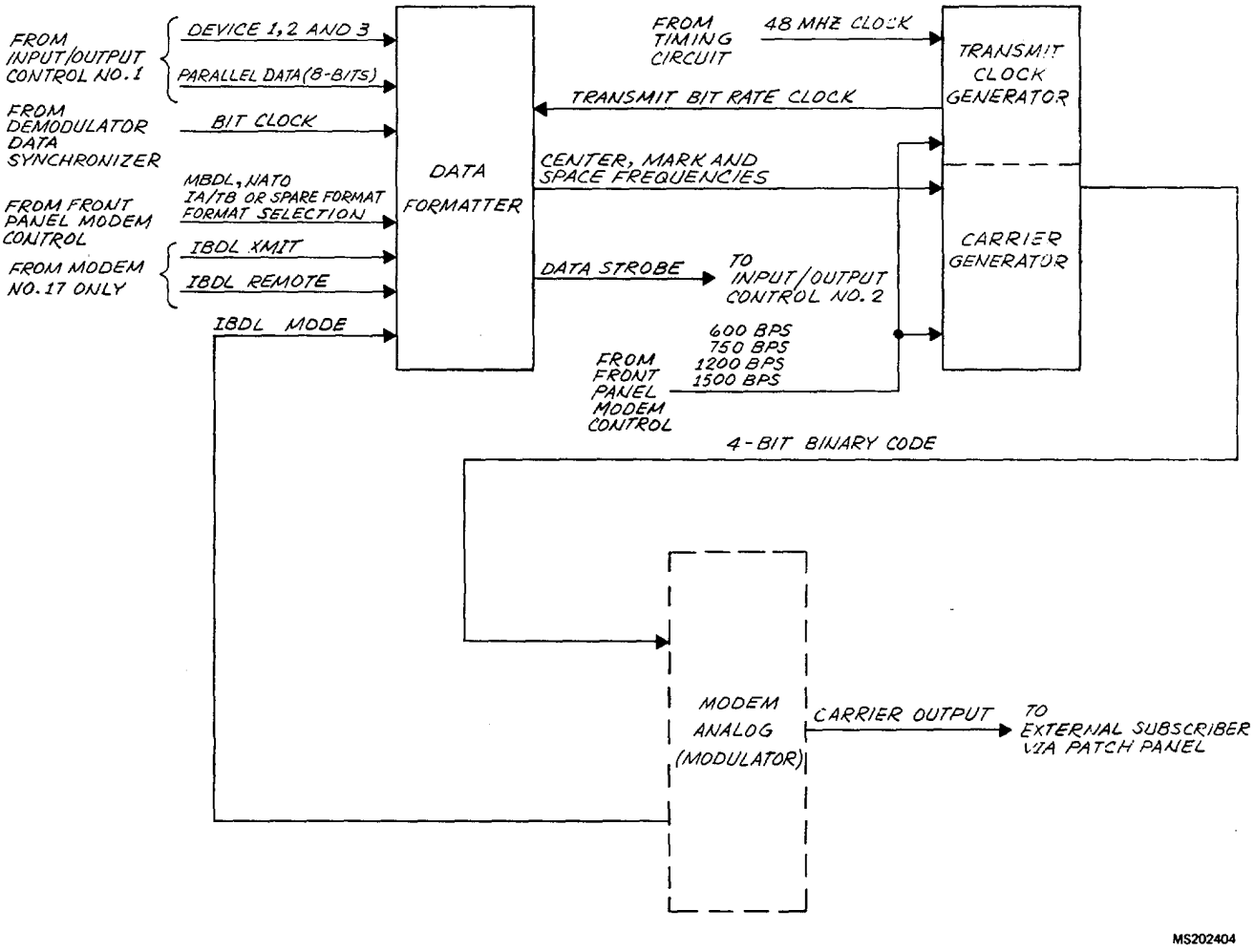


Figure 5-4. Typical Modulator Block Diagram

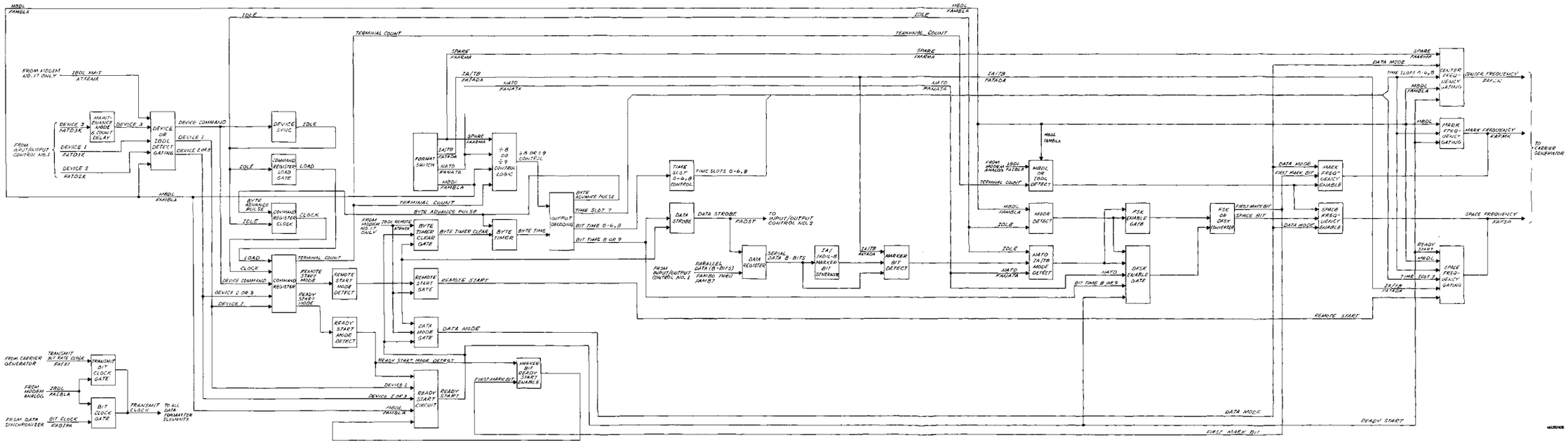


Figure 5-5. Data Formatter Block Diagram

5-29/(5-30 blank)

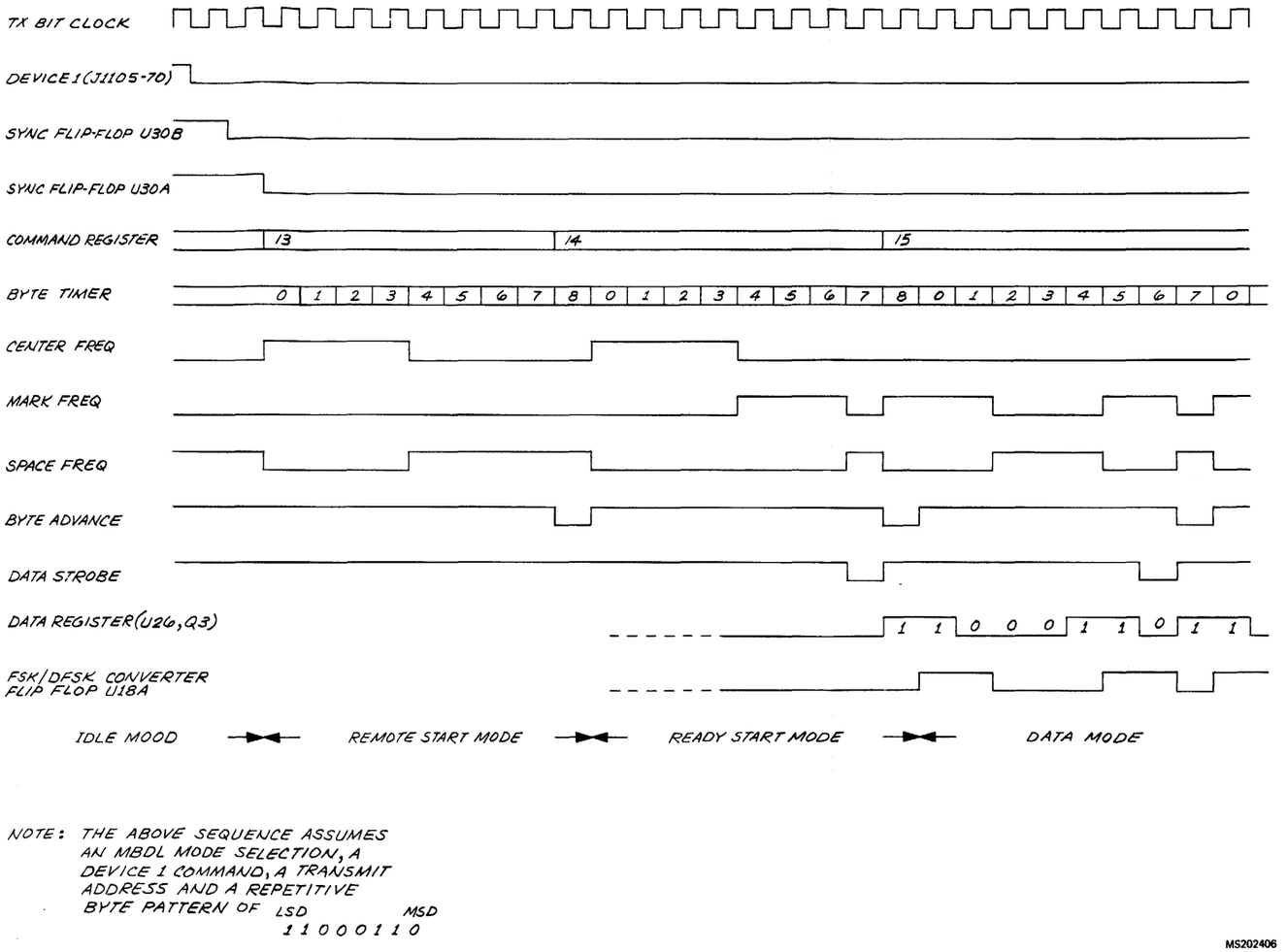


Figure 5-6. Typical Modulator Data Formatter Timing Diagram

Table 5-7. Mode Timing

Mode	Time period	fc	fm	fs	Data strobed
		t-4	0	0	1	1
IDLE		t-3	0	0	1	1
		t-2	0	0	1	1
		t-1	0	0	1	1
		t0	1	0	0	1
		t1	1	0	0	1
		t2	1	0	0	1
REMOTE		t3	1	0	0	1
START		t4	0	0	1	1
		t5	0	0	1	1
		t6	0	0	1	1
		t7	0	0	1	1
		t8	0	0	1	1
		t9	1	0	0	1
		t10	1	0	0	1
		t11	1	0	0	1
		t12	1	0	0	1
READY		t13	0	1	0	1
START		t14	0	1	0	1
		t15	0	1	0	1
		t16	0	1	0	0
		t17	0	1	0	1
	B0 1	t18	0	1	0	1
	B1 I	t19	0	1	0	1
DATA	B2 0	t20	0	0	1	1
	B3 0	t21	0	0	1	1
MODE	B4 0	t22	0	0	1	1
	B5 1	t23	0	1	0	1
	B6 1	t24	0	1	0	0
	B7 0	t25	0	0	1	1

(2) The device sync, upon receiving a device command, resynchronizes the incoming command with the current transmit clock. The inactive state of the device sync defines the idle mode for the remainder of the logic. After occurrence of the device 1 command, the device sync causes a binary 13 to be loaded into the command register. The command register is preset to 14 for both a device 2 or 3 command. Binary 13 contained in the command register clears the byte timer and enables the remote start mode. After the byte timer sequences through the remote start mode, a byte advance pulse steps the command register to binary 14. The byte timer sequences through the ready start mode and again supplies a byte advance pulse which steps the command register to binary 15. Binary 15 defines the data mode. The command register will remain in this condition for the remainder of the message.

(3) The byte timer controls the logic which generates the control and timing signals required to provide proper frequency output indications. Center frequency output gating is enabled when an MBDL mode is selected and a remote start mode or ready start mode is determined by the command register. Center frequency output gating develops a center frequency output from time slot 0 to time slot 3 of the current byte timing cycle. Mark frequency output gating develops a mark frequency from time slots 4 thru 6 and time slot 8. Space frequency gating develops the required space frequency at time slot 7 of the ready start mode. For MBDL select, the absence of terminal count from the command register allows output decoding to divide by nine for this particular timing sequence. At the count of nine, output decoding steps the command register to the data mode. At time slot 8, output decoding develops a data strobe which loads the 8-bit parallel data from input/output control no. 1 into the data register. The data strobe is also applied to input/output no. 2 for generating a transmit request to the IOM.

(4) After the data is loaded into the data register, the transmit clock steps the serialized data to the FSK or DFSK converter. Since the MBDL mode is currently selected, the data is passed unchanged and applied to the mark and space enable logic as the proper mark and space representation of the data. When a NATO format is selected, the FSK or DFSK converter toggles for a one and reflects no change for zero.

(5) Marker bits are used for the IA/TADIL-B, spare, and NATO formats as sync bits separating the data bytes and indicating the synchronization pattern. The IA/TADIL-B format uses a marker bit at the beginning and end of synchronization, whereas the spare and NATO formats use a marker bit only at the end of synchronization. The marker bit generator is used for the IA/TADIL-B format only. All other format marker bits are computer generated. The marker bit ready start enable is reset at the beginning of ready start and detects the first marker bit of the IA/TADIL-B format synchronization.

(6) The device 3 command is used for loop test. The maintenance mode 8 count delay provides a gap between loop test messages to eliminate message overlap which would result in loss of coherent data.

b. *Carrier Generator* (fig. 5-7, FO-3). The carrier generator converts the bit rate control indications and frequency controls into a 4-bit binary weighted signal for use by the modem analog. The + N selector decodes input levels representing frequency control (mark, center, and space frequencies) and bit rate select (600 bps, 1200 bps, 750 bps, and 1500 bps) information to determine the required division. The divisor preset code is then applied to the + 18 to + 44 variable counter. A + 8 fraction counter provides the feedback input control to the variable counter if the divisor is not a whole integer. For example, assume that a divisor of 29-1/8 is required to produce the correct carrier frequency. The variable counter is initially preset to perform a divide-by-29 operation. The fraction counter allows the variable counter to divide by 29 seven times, then forces the counter to perform a divide-by-30 operation on the eighth time. The average division factor for each operation is then 29-1/8. Refer to table 5-8 for the divisor operation relating to the different bit rate and frequency control. The + 18 to + 44 variable counter is a 256-bit counter that performs the actual division.

(1) The 16 state up/down counter converts the variable-frequency clock pulses from the variable counter into 4-bit binary-coded outputs representing the carrier frequency. Refer to figure 5-8 for up/down counter timing. The 16 state up/down counter is a - 32 up counter that initiates a down count every 16 clock times by gating the complement of the up count. The resulting 4-bit binary code outputs produced during the first 16 clock times are complementary to the binary outputs produced during the second 16 clock times. The 4-bit binary code represents the carrier frequency when a digital-to-analog conversion is performed. The resultant waveforms are represented as a modified staircase. The staircase waveform is then filtered by the modem analog circuit to provide the ultimate sinusoidal output.

(2) The transmit clock generator converts bit-rate input data into a variable division factor and produces square-wave signals at selected frequencies of 600 Hz, 1200 Hz, 750 Hz, and 1500 Hz.

5-11. Demodulator Detailed Description (fig. 5-9).

The demodulator consists of a frequency discriminator/ low pass filter, a data synchronizer, and a portion of the modem analog that is described in paragraph 5-12. The demodulator converts signals from FSK/DFSK carrier form to binary levels, recognizes message start preambles, performs receive timing synchronization, and controls data and information exchange with the input/ output control logic. The modem analog receives the carrier input from the external subscriber through the patch panel and converts the incoming sinusoidal signal into a square wave. The square wave (limiter carrier) is then applied to the frequency discriminator/low pass

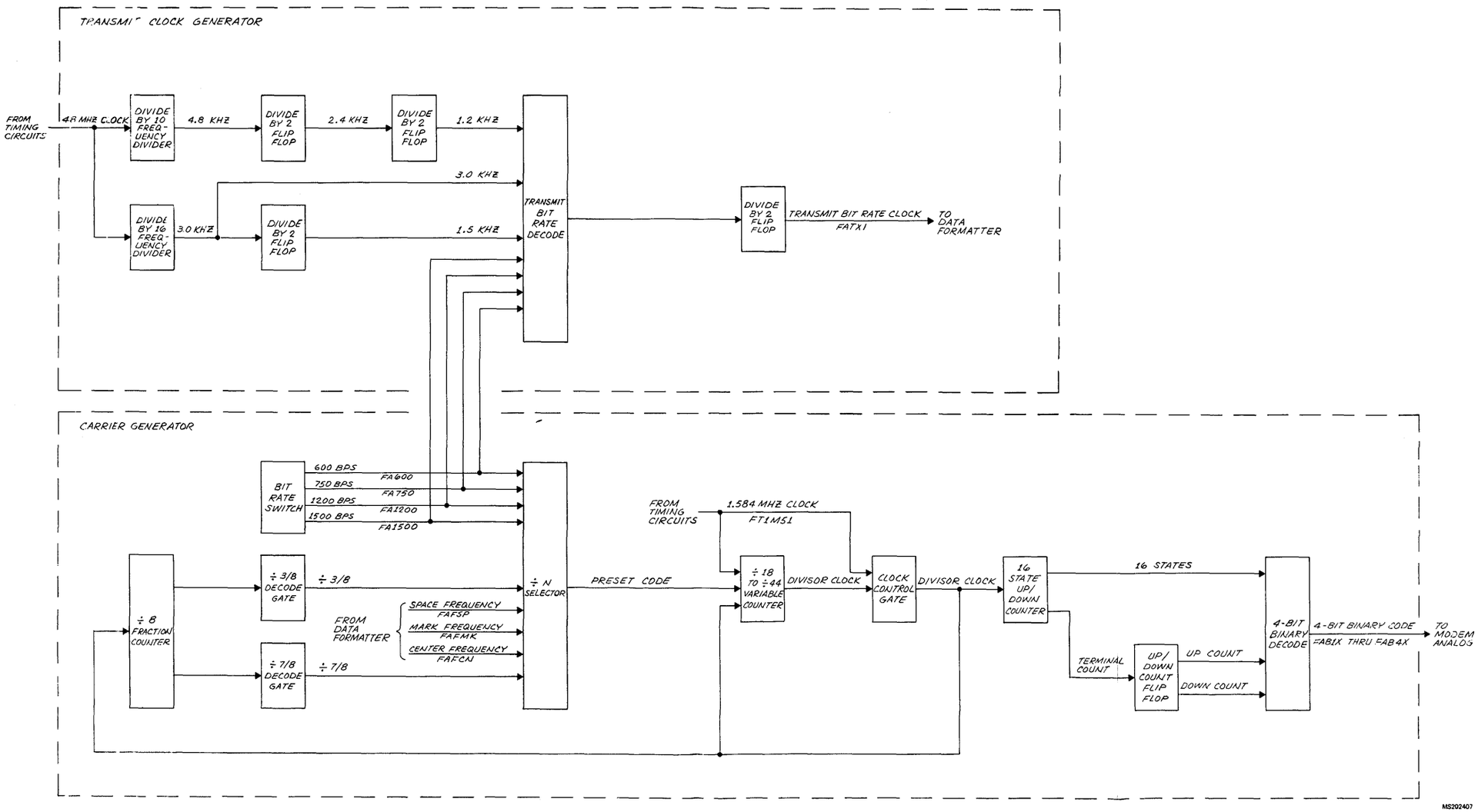


Figure 5-7. Carrier and Transmit Clock Generator Block Diagram

Table 5-8. Divisor Operation

Bit rate (bps)	Frequency control fm	fc	fs	Carrier req Hz	Divisor	Variable counter preset code (msb) A B C D E F G H	Fraction counter feedback
	1	0	0	1300	38	0 1 0 1 1 0 1 1	X
600	0	1	0	1500	33	1 1 1 1 1 0 1 1	X
					29	1 1 0 0 0 1 1 1	7
	0	0	1	1700	(29-1/8)		
					30	0 1 0 0 0 1 1 1	1
	1	0	0	1125	44	0 0 1 0 1 0 1 1	X
750	0	1	0	1500	33	1 1 1 1 1 0 1 1	X
					26	0 1 1 0 0 1 1 1	5
	0	0	1	1875	(26-3/8)		
					27	1 0 1 0 0 1 1 1	3
	1	0	0	1300	38	0 1 0 1 1 0 1 1	X
					29	1 1 0 0 0 1 1 1	7
1200	0	1	0	1700	(29-1/8)		
					30	0 1 0 0 0 1 1 1	1
					23	1 0 0 1 0 1 1 1	3
	0	0	1	2100	(23-5/8)		
					24	0 0 0 1 0 1 1 1	5
	1	0	0	1125	44	0 0 1 0 1 0 1 1	X
					26	0 1 1 0 0 1 1 1	5
1500	0	1	0	1875	(26-3/8)		
					27	1 0 1 0 0 1 1 1	3
					18	0 1 1 1 0 1 1 1	1
	0	0	1	2625	(18-7/8)		
					19	1 0 1 1 0 1 1 1	7

filter. The frequency discriminator converts the half cycle between the high and low carrier frequency into 16 binary levels. The low-pass filter converts the 16 binary levels back to binary data signals and smooths out any noise spikes. The binary data signals represent low pass filter data and center frequency applied to the data synchronizer. The advance/retard disable signal represents the carrier frequency and is used by the data synchronizer for MBDL format synchronization. The data synchronizer receives the binary data and performs receive timing synchronization, start-of-message detection, and serial-to-parallel data conversion. The data synchronizer function is controlled by message format selection, bit rate selection, device 1 and 3 commands, and EOB signals. The device command and EOB signals cause the data synchronizer to sense the start of a new message. After the message start is detected, the data that follows is transferred to input/output control no. 2 in 8-bit bytes, along with a data available signal which indicates that the bytes is ready for transfer. The demodulator busy signal indicates that the data synchronizer is busy receiving new data and no data is available for transfer to input/output control no. 2. During IBDL mode, a dedicated modem (no. 17) is actuated, and utilizes only the MBDL format. The bit clock from the data synchronizer and all modem no. 17 associated signals are applicable to the IBDL mode of operation. Refer to section IV for IBDL mode description.

a. Frequency Discriminator/Low Pass Filter (fig. 5-10, FO-4). The frequency discriminator/low pass filter measures the time interval between the transitions of the limited carrier waveform and determines whether the current bit is a center, mark, or space frequency. The frequency disciminator develops a binary weighted value that represents the one-half cycle difference between the upper carrier and the lower carrier of the input waveform. A succession of these binary weight values is effectively integrated by the low pass filter in order to

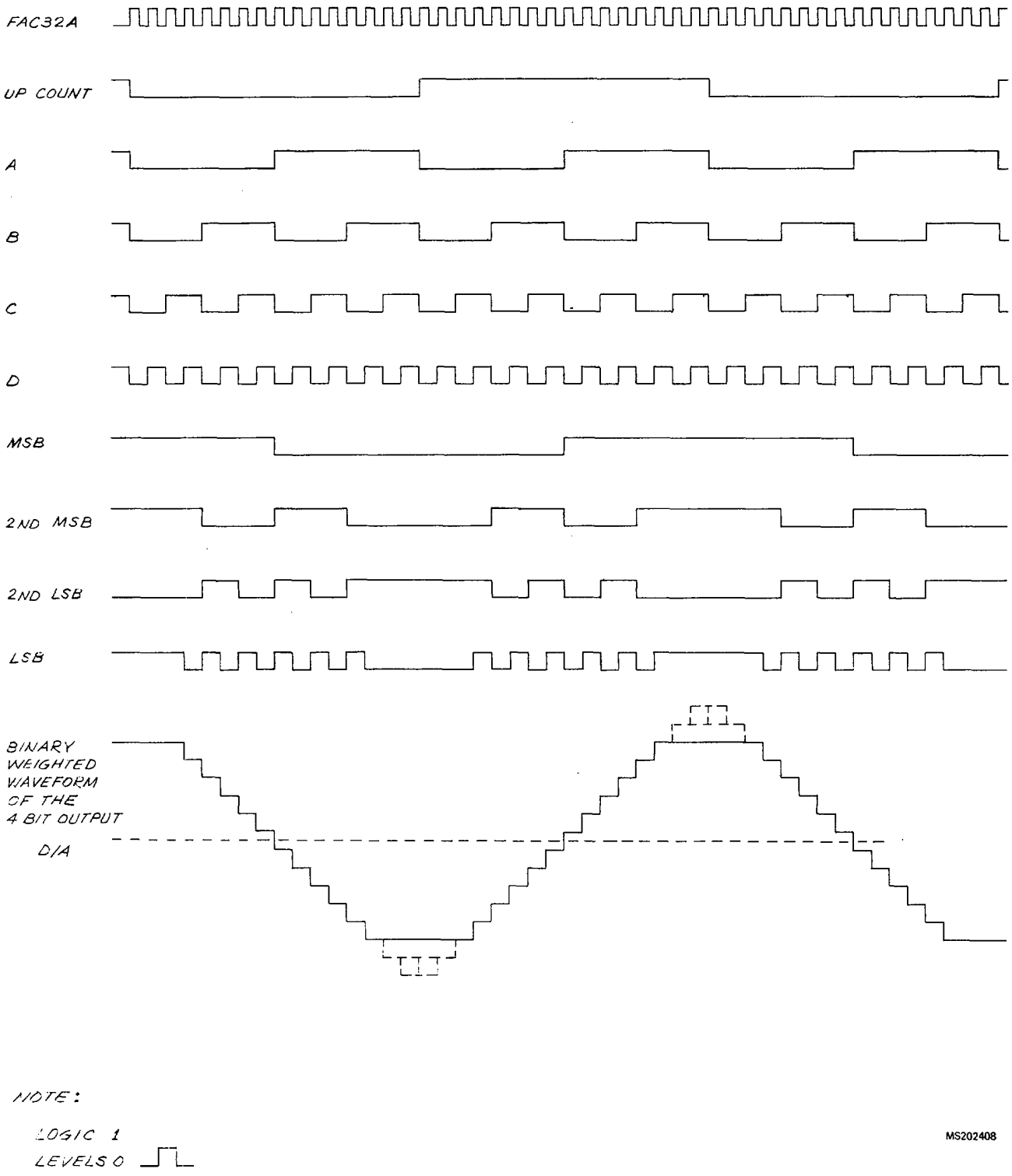


Figure 5-8. Carrier Generator 16-State Up-Down Counter

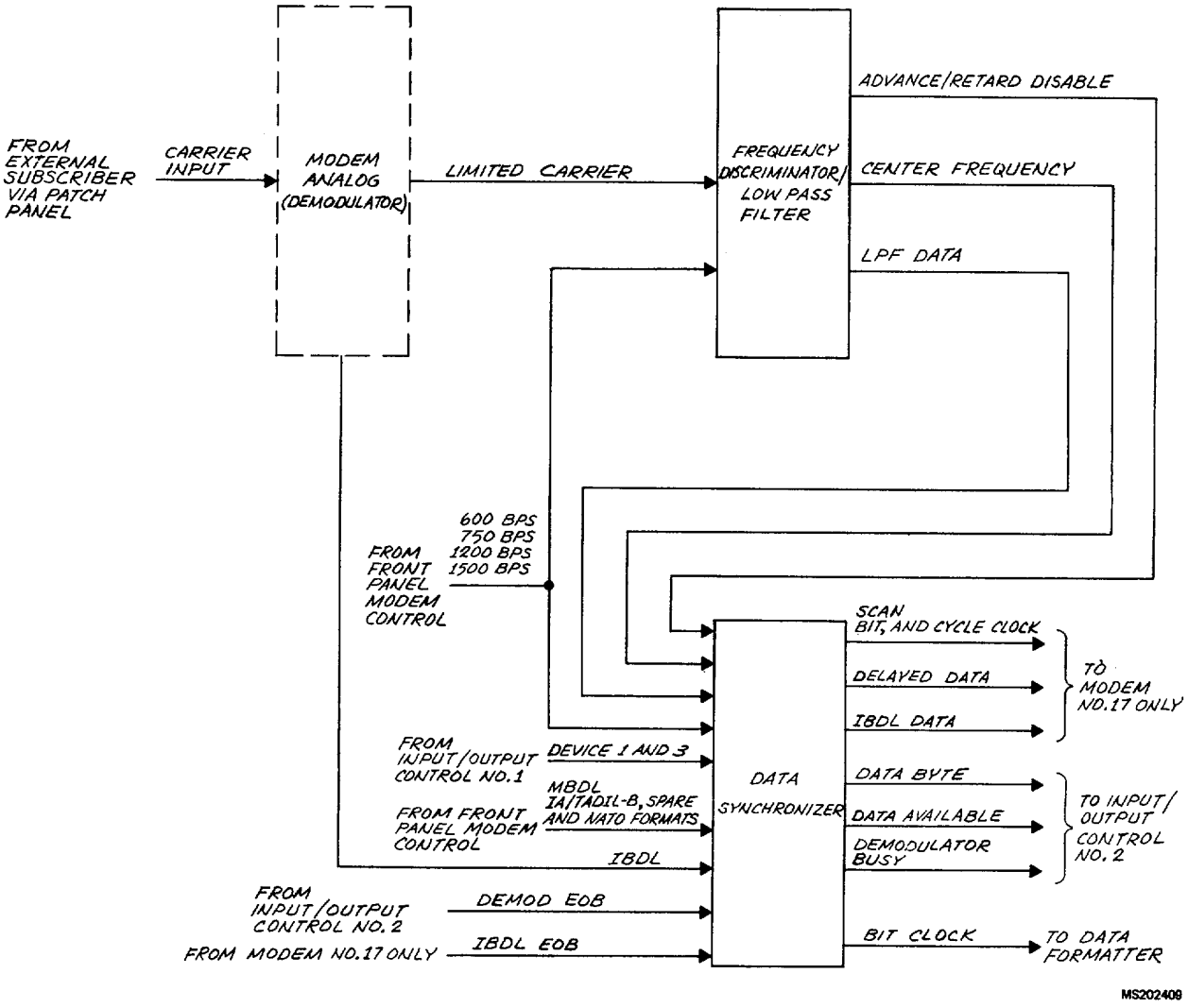


Figure 5-9. Typical Demodulator Block Diagram

recover the actual data and the current center frequency. A timing diagram of discriminator operation is shown in figure 5-11. Initially the discriminator is mechanized to determine the half cycle interval of the center frequency by counting down the 1.584 MHz clock. The actual count values are determined by the bit selection switches applied to the delta time control. For purposes of this description, the modem is using a 750 bit-per-second rate and frequencies are mark, 1125, center, 1500, and space, 1875. The full cycle times for the frequencies are 888, 666, and 533 microseconds, respectively. Refer to figure 5-12 for discriminator time and frequency relationships. The time will be counted out by the clock generator counter and decoded by the mark half cycle decode.

(1) The frequency disciminator circuit is initialized each time the transition detector indicates that a high to low or low to high transition has occurred at the limiter carrier input. As shown in figure 5-10, any transition which is detected by the zero-crossing gate clears the delta time counter and initializes the clock generator counter. Refer to figure 5-13 for frequency half cycle and delta time counter relationships. The clock generator counter will cycle to a full count of 255 overflow, step the delta time counter to the ONE state and then commence to recycle. When the clock generator counter reaches a count of 170, which is decoded by the mark half cycle decode, the end of the zero-crossing window or a mark frequency half cycle is detected. The zero-crossing window provides noise and high frequency rejection by preventing any zero crossing short of a mark half cycle time (268 usec for 750 bps) from disturbing the holding register. Thus any short mark zero crossing occurring during a center or space bit time will restart the discriminator but will not load all zeros (representing a mark frequency to the low pass filter) in the holding register. A short mark zero crossing occurring during a legitimate mark bit time will also be ignored. When the next half cycle reflects a long mark half cycle, the discriminator will restart and load all zeros into the holding register from the delta time counter. A long mark half cycle will occur, from a 171 to 182 clock generator count, which reflects a modulo 12 from delta time control.

(2) The clock generator counter now continuously cycles on modulo 12, with each cycle stepping the delta time counter. When the delta time counter reaches a count of 8, delta time control will drive the clock generator counter at modulo 16. The center frequency half cycle is defined as a zero crossing occurring at a count of 6, 7, 8, or 9 of the clock generator counter. The center frequency mean value is stored in the holding register and is used as an advance/retard disable signal to the data synchronizer for MBDL format synchronization.

(3) When the delta time counter reaches a count of 12, delta time control drives the clock generator counter at modulo 24. The mark frequency half cycle is defined as a zero crossing when the delta time counter reflects a count of 15. The detection of the transition reinitiates the discriminator for the next half cycle detection sequence and loads the delta time counter contents (all ones) into the holding register. The value is now available to the low pass filter for further processing.

(4) The sample clock generator provides the sampling bit time clock rate for the low pass filter. The sample clock generator divides the input clock (1.584 MHz) by 4 or 8 and 12 or 14 depending upon the bit rate selected. Refer to table 5-9 for sampling bit time clock rate calculations. The low pass filter samples the input full cycle frequencies at a minimum of 8 samples/per space, 10 samples/per center, and 12 samples per mark.

(5) The low pass filter is logically mechanized to perform the equation bn + 1 = bn + 1/8(a - bn). The a defines the current value in the holding register, bn defines the last value computed, and bn + 1 defines the new value computed. Subtracting a - bn is implemented by inverting the subtractor (4 most significant bits of the accumulator) and forcing a one in the least significant bit of the adder which provides the 2's complement. The resultant subtraction is divided by 1/8 and is implemented by shifting the subtractor (and thus the difference) three places to the right (input to adder). The bn is then added to the positive or negative result of the division by using the carry bits from the least significant digit adder and the subtractor to increment or decrement the three most significant bits of the accumulator. The three permutations of increment/decrement conditions are as follows:

(a) No adder carry and negative difference (subtractor carry zero). Add all ones to accumulator most significant bit, which effectively decrements the value by one.

(b) Either adder carry or positive difference (the absence of one cancels the other). Add all ones to accumulator most significant bit with carry, which effectively adds all zeros or no change.

(c) Both adder carry and positive difference. Add all zeros with carry, which effectively increments the accumulator value by one.

Table 5-9. Sample Clock Generator Sampling Bit Time Clock Rate Calculation

Bps rate	Frequency division	usec/ sample	Sample bit time
600	112	70.67	23
750	96	60.57	22
1200	56	35.33	23
1500	48	30.28	22

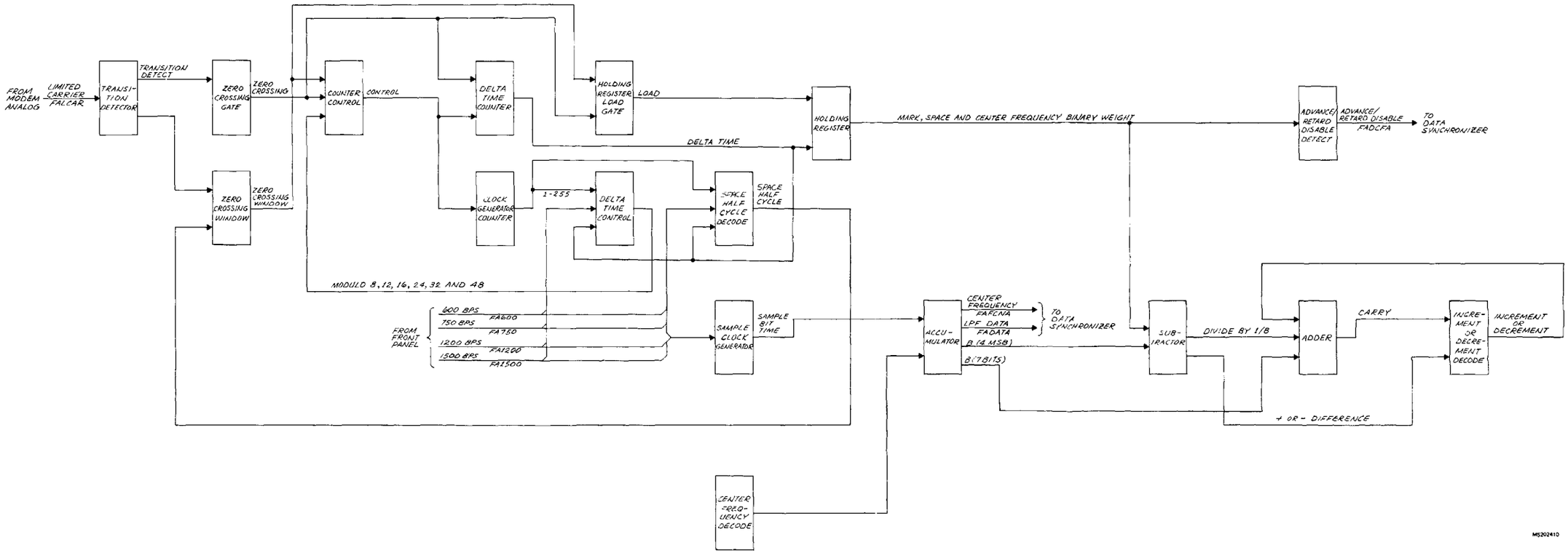


Figure 5-10. Frequency Discriminator/LP

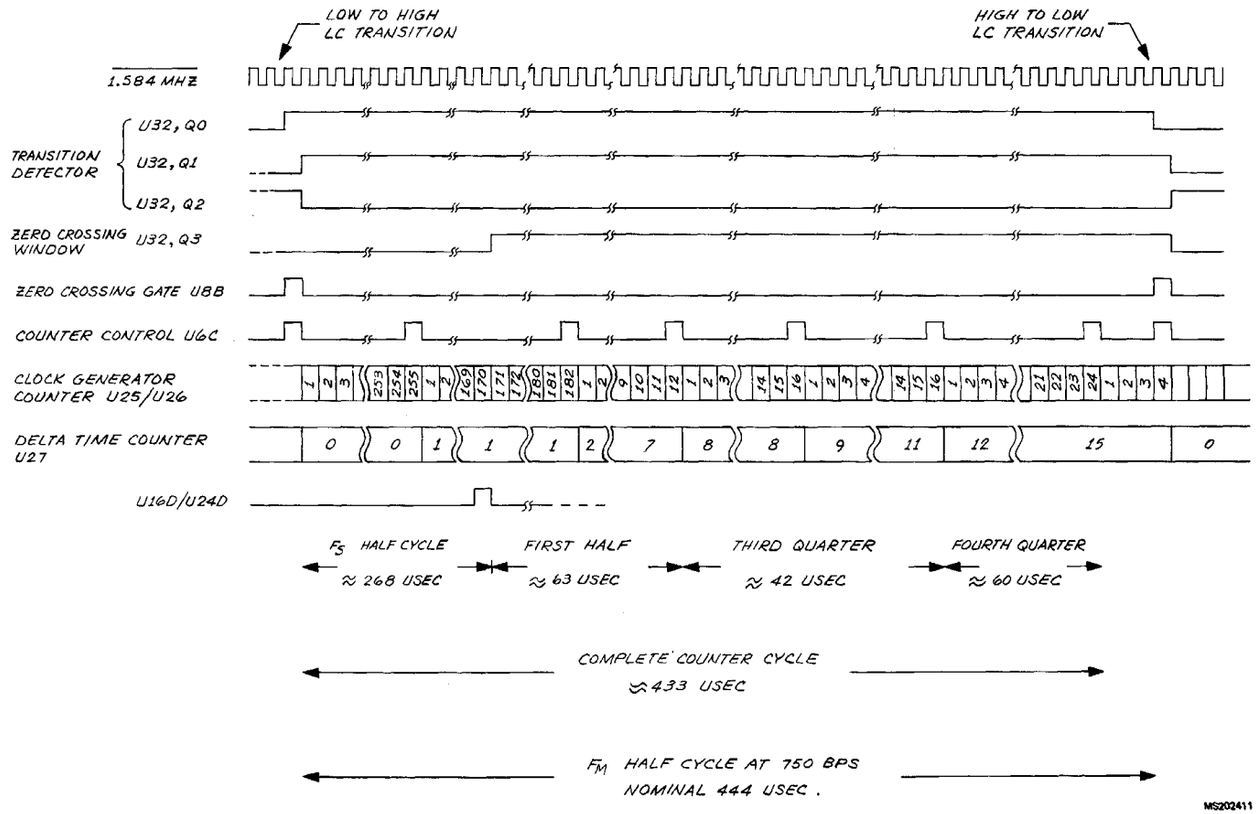


Figure 5-11. Typical Discriminator Timing

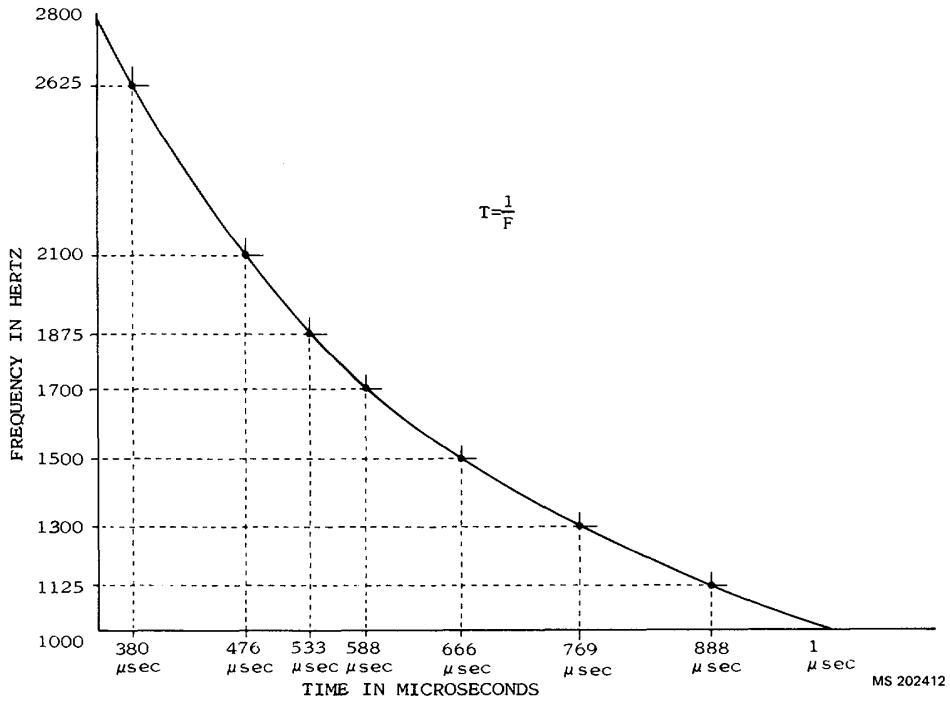


Figure 5-12. Discriminator Time and Frequency Relationship

(6) The carrier frequency is detected by the mean code contained in the accumulator.

b. Data Synchronizer (fig. 5-14, FO-5). The data synchronizer receives low-pass filter data and synchronizes the data with internal timing, detects the start of message, and converts the serial data into the parallel byte form required at the output interface. The data synchronizer performs two methods of data synchronization, the advance/retard method, and the MBDL mode synchronization method. The operation of the data synchronizer is dependent on the bit rate currently selected. The bit rate selected for this description will be 750 bps.

(1) The advance/retard data synchronization method is used for all modes, with the exception of the MBDL mode of operation. Refer to figure 5-15 for advance/retard timing. The current bit rate is determined by the bit selection inputs to the frequency divider control, which supplies a preset code to the frequency dividers. The preset code determines the divider ratio for the different bit rates. Refer to table 5-10 for the frequency divider ratio per bit rate selection. The bit and cycle clock control also further divides the frequency by two. The division is accomplished by presetting the frequency divider A to 12 and frequency divider B to 8 and allowing the frequency dividers to overflow. The advance/retard register detects data transitions and determines whether the transition is high or low. The current state of the advance/retard register is compared at approximately each bit time with the condition of frequency divider B in order to determine whether data transmission is early; late, or on time. If the data transition is early or late, frequency divider B will be retarded or advanced as required. The primary function of the circuit is to ensure that the bit and cycle control reflects a negative transition for each crossover of the input data. As shown in the timing diagram, frequency divider A continuously cycles from count 12 thru count 15. Each time frequency divider A reaches terminal count, a scan clock signal will step frequency divider B. Frequency divider B will normally cycle from count 8 thru count 15 and overflow. If the input data is precisely in sync with the output clock, the transition would occur at the point where both frequency dividers are full and the circuit would commence to recycle.

(2) Each time frequency divider B reaches count 15, the frequency divider B load enable will reinitialize the frequency divider. Count 15 also allows the bit and cycle control to be toggled by the scan clock pulse from frequency divider A.

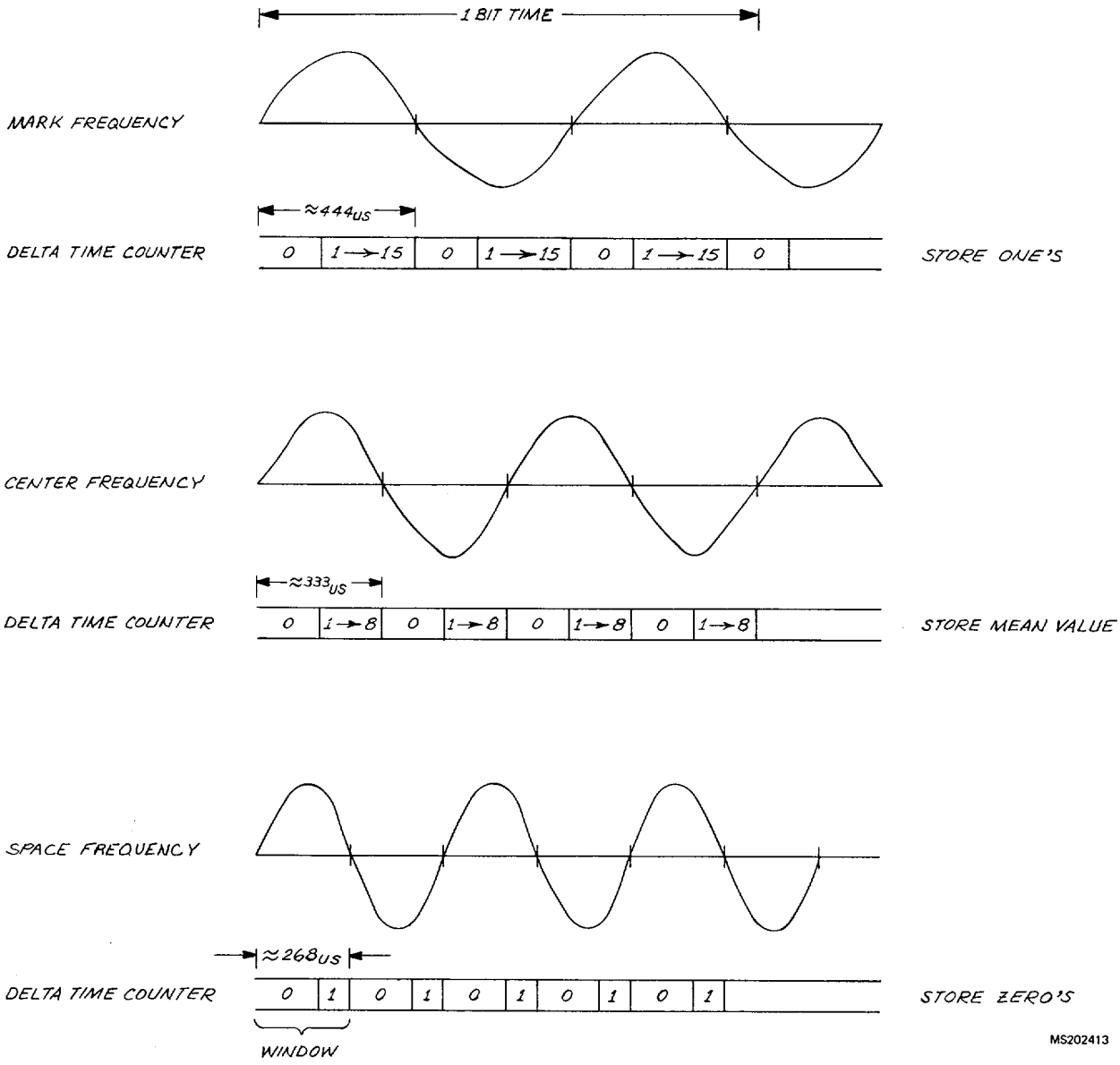


Figure 5-13. Frequency Half Cycle and Delta Time Counter

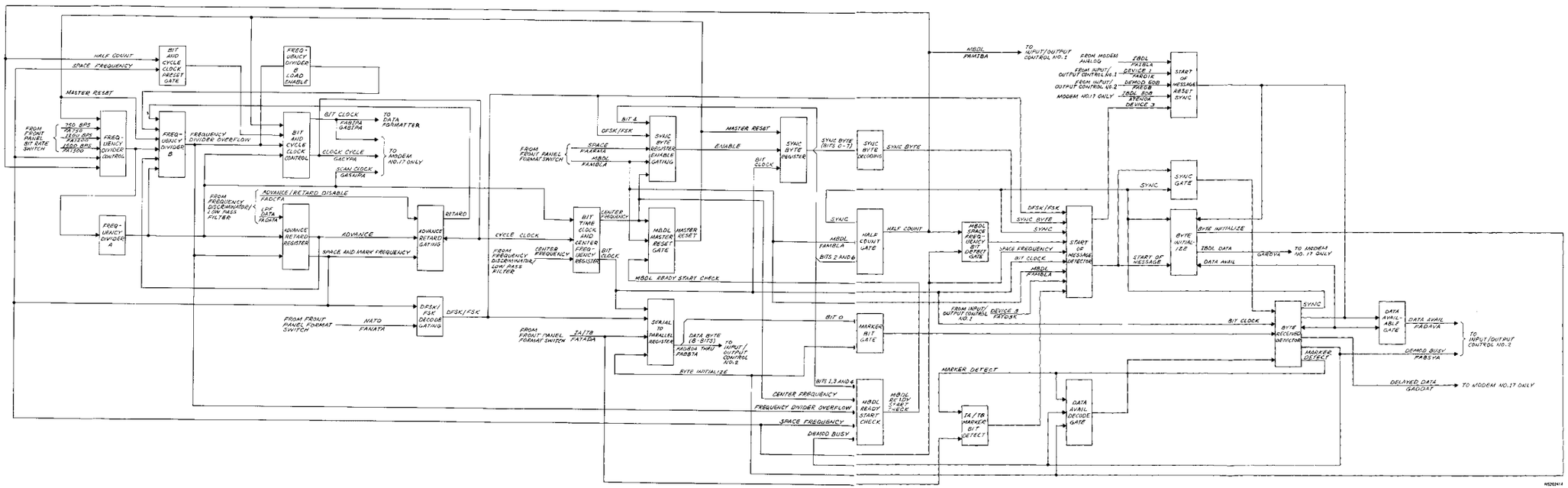


Figure 5-14. Data Synchronizer, Block Diagram

5-47/(5-48 blank)

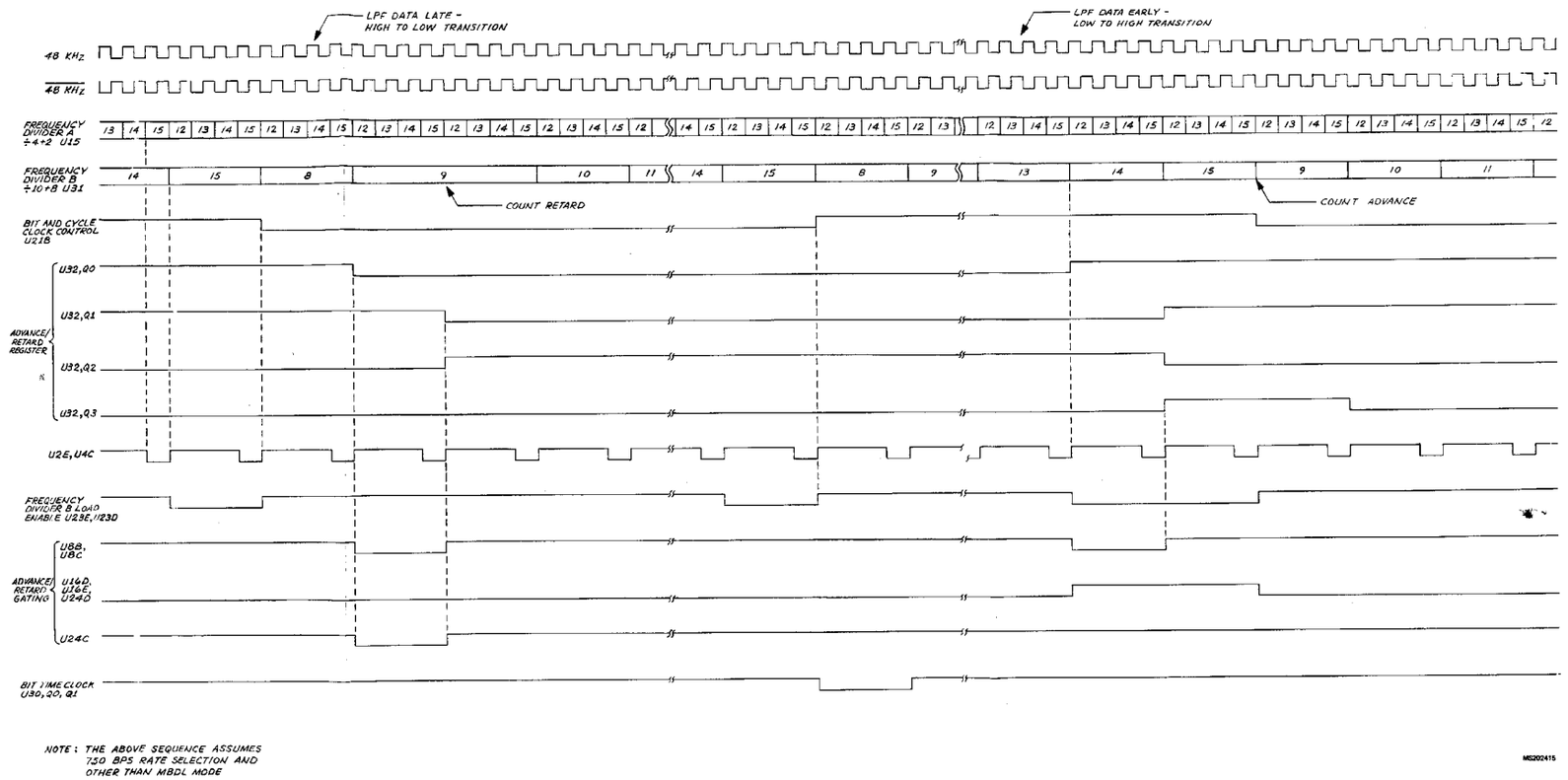


Figure 5-15. Data Synchronizer Advance/Retard Timing

Table 5-10. Frequency Divider Ratio

Bit rate	Frequency divider A	Frequency divider B	Bit and cycle clock control	Total division
600	4 (12 KHz)	10 (1200Hz)	+ 2 (600 Hz)	80
750	+ 4 (12 KHz)	8 (1500 Hz)	+ 2 (750 Hz)	64
1200	+ 2 (24 KHz)	+ 10 (2400 Hz)	2 (1200 Hz)	40
1500	+ 2 (24 KHz)	- 8 (3 KHz)	2 (1500 Hz)	32

(3) A high-to-low transition occurring on LPF data will reset the advance/retard register and will be detected by advance/retard gating. The coincidence of the transition and the reset of the bit and cycle control allows a retard signal from advance/retard gating to prohibit the next clock from advancing frequency divider B. Frequency divider B will instead be retarded by one count. The frequency divider now will cycle up to maximum count as previously described and will set the bit and cycle clock control, reinitializing the circuit.

(4) When the data transition occurs early, the transition occurs before frequency divider B reaches full count and the bit and cycle control is set. The next count 15 from frequency divider A allows the advance/retard register to advance frequency divider B one additional count. The frequency dividers will then continue to cycle in the usual manner. If clock phasing is not corrected by adding one additional count, frequency divider B will continue to hunt by advancing one or more counts until proper synchronization is obtained with the input data.

(5) The MBDL mode synchronization method is used when the MBDL format is selected. Since the MBDL format involves a discrete synchronization pattern (four bits center frequency, three bits mark frequency, one bit space, and one bit mark), the pattern is used to synchronize the bit clock timing and to detect the start of a message. The advance/retard method is disabled by an advance/retard signal from the frequency discriminator during MBDL synchronization.

(6) The bit time clock and center frequency register detects a center frequency and enables the MBDL master reset gate. Refer to figure 5-16 for MBDL ready start detect timing. The MBDL master reset gate resets the sync byte register, the bit and cycle clock control, and the MBDL ready start check circuit. The MBDL master reset gate also forces a binary 14 into frequency divider B. Frequency divider B then cycles through, developing a bit time clock from the bit time clock register that forces a ONE into the sync byte register.

(7) The MBDL ready start check detects center frequency and the first space frequency occurring at the proper time for verification of the MBDL ready start pattern. Refer to figure 5-17 for complete MBDL data synchronization and processing timing. Frequency divider B continues to recycle with each bit time clock stepping a one into the sync byte register. At the time the third mark frequency is expected to appear on the data input, the half count gate forces a two instead of a four into frequency divider A each cycle. Halving the counting speed of frequency divider A allows the MBDL space frequency bit detect gate to sense the start of a MBDL message. After the start of a message is detected, the serial-to-parallel register is initialized. The bit zero from the serial-to-parallel register is used as a marker bit to notify the appropriate logic when the full 8-bit byte is loaded into the register and is ready for transfer. Since the NATO format is not selected, the mark frequency signal from the advance/retard register is used to step the inverted data into the serial-to-parallel register.

(8) The start of a message also produces a sync output signal from the byte received detector, which indicates that the current start of message is detected and that the message is being processed. As shown is figure 5-17, the occurrence of the marker bit also generates a data available signal from the byte received detector to input/output control no. 2, indicating that a byte is available in the serial-to-parallel register for transfer to the interface. The data available signal also allows the byte initialize circuit to reinitialize the serial-to-parallel register for the next byte. The conversion and transmission of the byte data will continue as described until the DEMOD EOB signal is received by the start of message reset sync circuit, which resets the byte received detector.

(9) When the spare format is selected, the sync byte register enable gating steps the sync byte register as long as center frequency is present. The detection of eight

bits of center frequency allows sync byte decoding to enable the start of message detector, which initializes the start of a message as previously described for the MBDL format.

(10) For NATO or IA/TB formats, the sync byte register enable gating steps the sync byte register as long as zeros are on the input data line. The proper number of contiguous zeros in the synchronizing pattern allows sync byte decoding to initiate the start of message detector as previously described. The DFSK/FSK decode gating is used during the NATO format to invert the data and step the data into the serial-to-parallel register.

5-12. Modem Analog Detailed Description (fig. 5-18, FO-3). The modem analog circuit is used in conjunction with other modem circuits to perform FSK/DFSK modulation and demodulation. The modulation section provides digital-to-analog conversion and filtering for FSK/DFSK modulated input signals, and the demodulation section provides bandpass filtering and limiting to FSK/DFSk carrier signals prior to actual demodulation. A loop test circuit is also provided to permit back-to-back testing of the modem.

a. Modulation Section;. The modulation section consists of a digital-to-analo, (D/A) converter, low pass filter, buffer amplifier, line coupler, and attenuator switch located on the modem control panel. The D/A converter accepts 4-bit binary code data from the carrier generator or from the IBDL circuit (during the IBDL mode of operation) and converts the data into an equivalent analog signal. Due to the weighting of the binary input code by the D/A converter and the repetition rate, the resulting output approximates a trapezoidal waveform that represents the selected carrier frequency. The low pass filter smoothes the output waveform, transforming the waveform into a sinusoidal signal. The output from the low pass filter is connected in parallel to an external variable attenuator, which controls the modulated output level in approximately 1 dbm steps from 0 to -20 dbm, when transmitted into a 600-ohm load. The buffer amplifier provides the power gain required to drive the output line coupler. The line coupler provides dc isolation, impedance matching, and lightning protection. The modulated output from the buffer amplifier is also coupled to a loop test switch, to permit loop testing of the modem in the back-to-back mode. The loop test switch is described in the demodulation section.

b. Demodulation Section. The demodulation section consists of a line coupler, loop test switch, bandpass filter, limiting amplifier, and level shifting comparator. The FSK/DFSK carrier input is coupled by a line coupler to the loop test switch. The line coupler provides impedance matching, lightning protection, and dc isolation. The loop test switch permits selection of either the carrier input or the modulated signal from the modulation buffer amplifier (loop test). The device 3 control signal provides the selection for the loop test switch, the output of which is applied to a bandpass filter. Low-pass and high-pass sections in the filter are controlled by 1200 bps and 1500 bps signals through a control gate. The low pass filter cutoff frequency is determined by the bit rate selected. When bit rate 600 or 750 is selected, the upper cutoff frequency is 2 kHz. When bit rate 1200 or 1500 is selected, the upper cutoff frequency is 3 kHz. The cutoff frequency of the high pass filter is 1 kHz for all bit rates selected. The bandpass filter improves the signal-to-noise ratio by restricting the noise bandwidth of the input signal. The output from the bandpass filter is applied to a limiting amplifier which converts the sine-wave input into a square-wave output and removes any residual amplitude modulation from the received signal. The square wave output is supplied to a level-shifting comparator to minimize circuit noise and produce output voltage levels that are compatible with subsequent logic. The square wave signal is then supplied to the frequency discriminator/low pass filter for processing and to the data bus gate. When the channel select and MBDL signal is active, the data bus signal is supplied to all modems. The channel select and MBDL signals will also supply an in use bus signal to the IBDL circuit when the power status signal is active.

5-13. Input/Output Control No. 1 Detailed Description (fig. 5-19, FO-6). Input/output control no. 1 accepts the parallel data bytes from the input/output multiplexer (IOM), decodes the commands, device, and address information, and generates control signals which permit the data to be processed by the modem. Refer to figure 5-20 for typical input/output control timing. The following description assumes that the input data reflects a transmit address, a device 1 command, and normal operation (no parity error, TX timeout, etc.).

a. Temporary storage of all data or command words from the IOM is provided by nine input data latches (8-bit data byte plus 1-bit parity). Input data to the input data latches is a negative-going pulse with a nominal pulse duration of 180 nanoseconds. The occurrence to a one on any one or on a combination of the input data lines initiates a timing sequence during which the input data is interpreted and required control functions are generated. The maximum rate at which data is sent from the IOM is 1.58 mHz. The timing sequence is performed by the timing counter. The timing counter will reset after time slot 4 if data is not sensed. Time slot 4 acts as a feedback to the data detection circuit and provides an enable or disable, depending on the presence of data, to the transmit buffer. Time slots 3-5 are used to control the storage of data in the transmit buffer. If no parity error or transmit timeout is detected, time slots 3-5 will allow the data to be stored. At time slot 5, a signal is sent to input/output control no. 2 for generating a transmit EOB. The effect of the transmit EOB is to cause the modulator to cease requesting data from the IOM. Time slot 6 is used in the command decode section to enable storage of a particular command received. The timing counter, upon reaching time slot 7, resets all the input data latches. All timing signals are distributed to

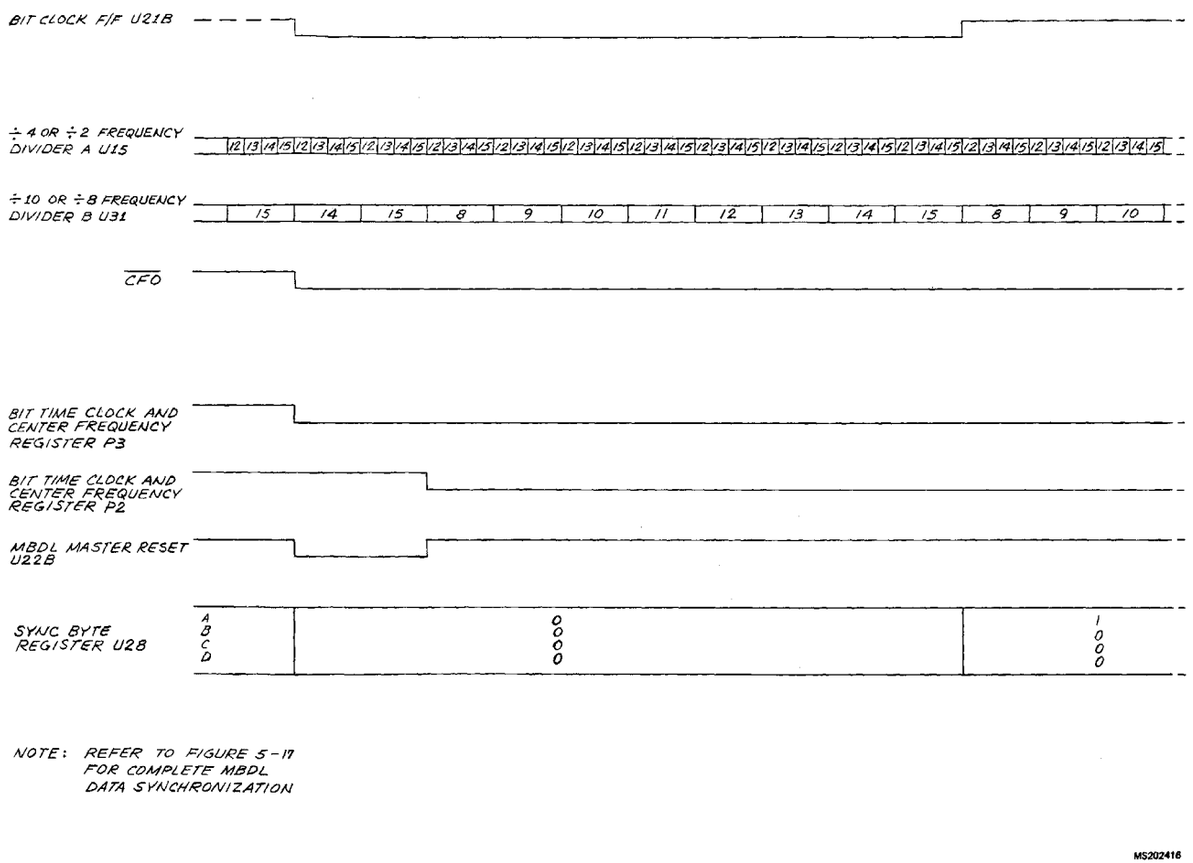


Figure 5-16. Data Synchronizer MBDL Start Detect Timing Diagram

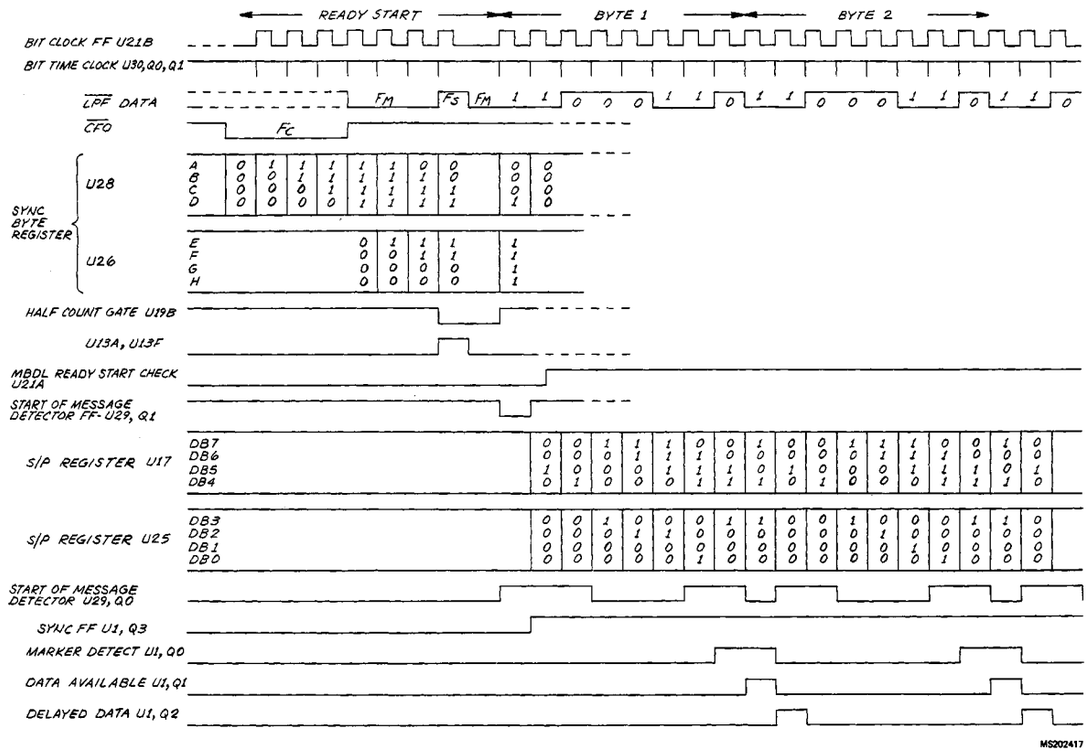


Figure 5-17. MBDL Data Synchronization and Processing Timing Diagram

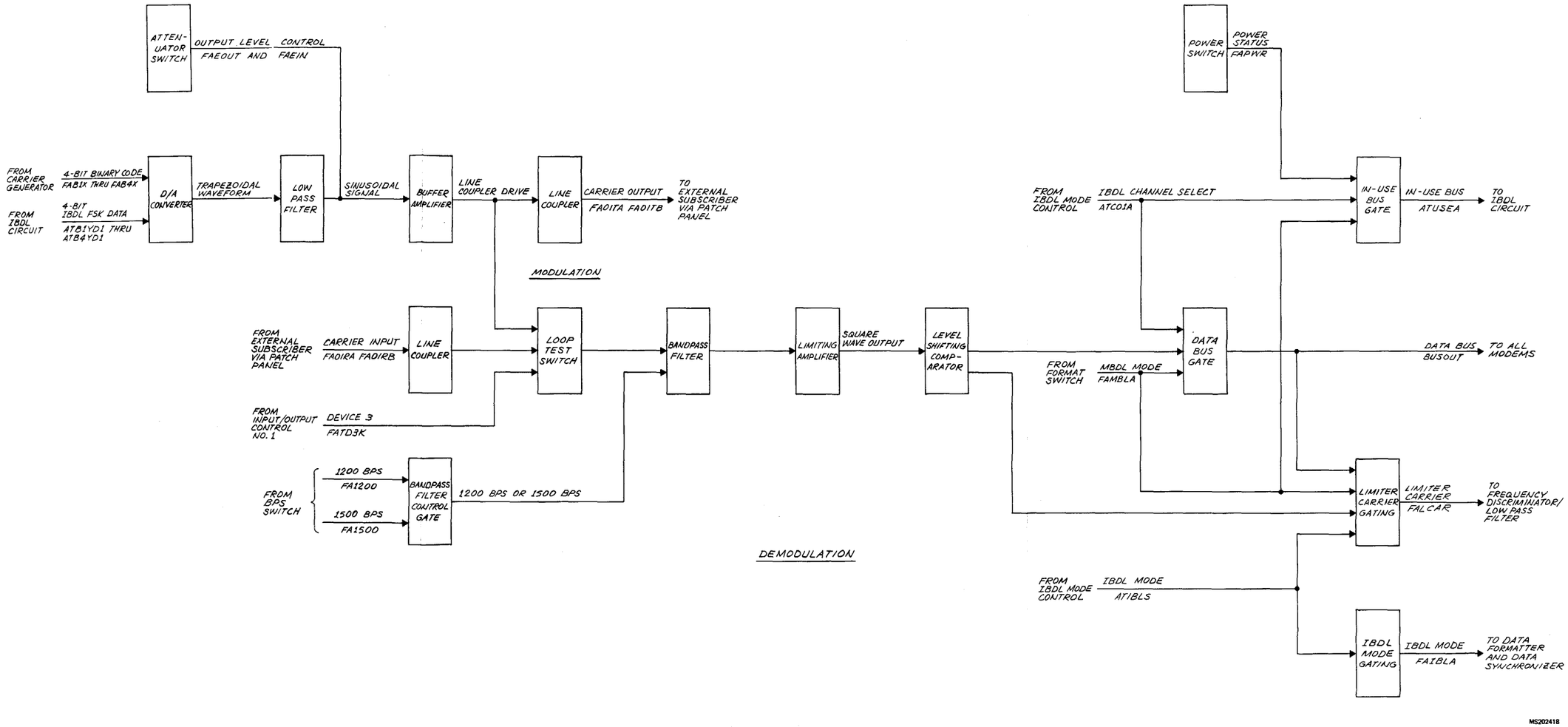


Figure 5-18. Modem Analog Block Diagram

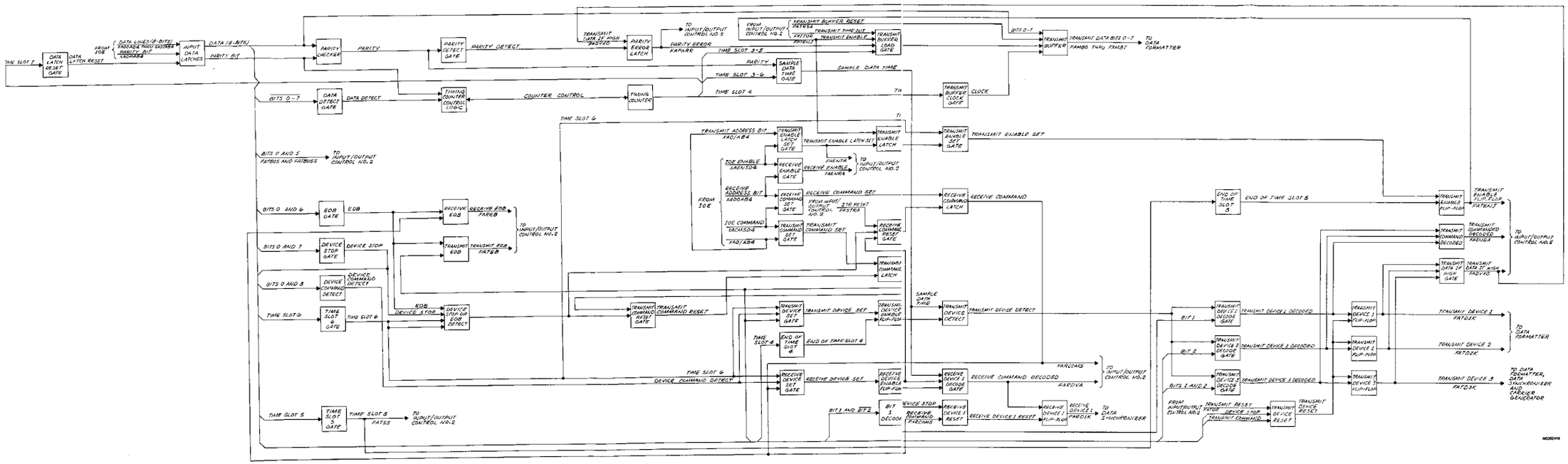


Figure 5-19. Input/Output Control No. 1 Block Diagram

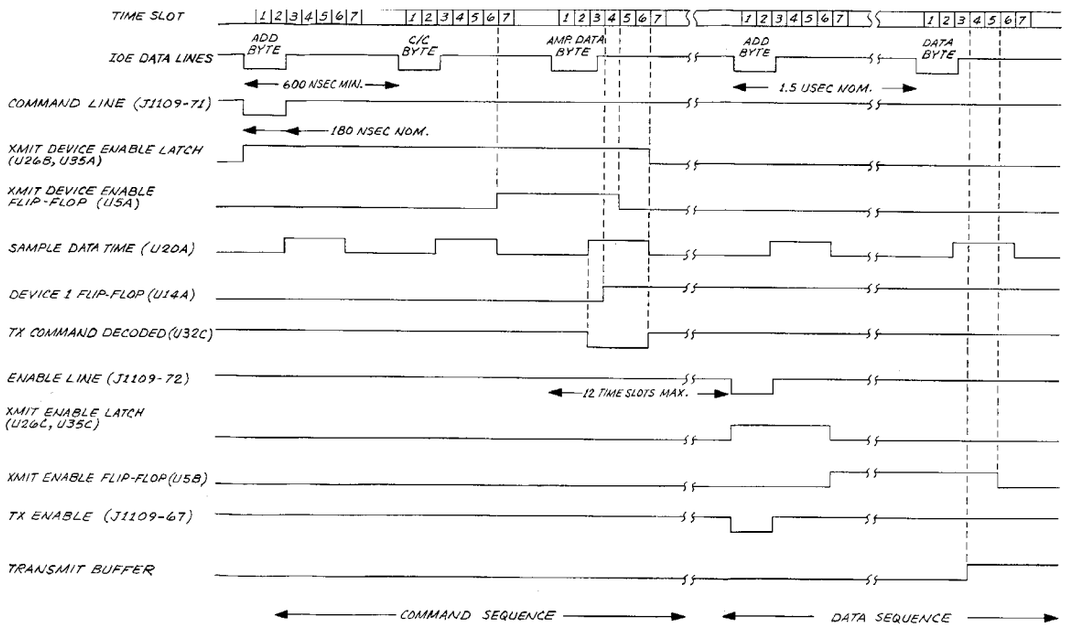


Figure 5-20. Typical Input/Output Control No. 1 Timing

the logic in order to process the input bytes. Since the input data is asynchronous, the timing counter can produce a 6 or 7 bit cycle, depending upon the input data phase relationship.

b. Commands to receive or transmit are logically implemented in the same manner; therefore, only the transmit command will be described. The transmit command requires two data bytes from the IOM. The first data byte contains a single bit (transmit address bit) which is active and specifies the addressed modem. The transmit address bit is supplied to the input data latches to initiate a timing sequence, and to the transmit command logic to initiate a transmit command. Coincident with the transmit address bit is a command signal. The simultaneous appearance of a transmit address bit and command signal causes the transmit command set gate to set the transmit command latch. The next data byte specifies the device command defined by bits 0 and 3 from the input data latches. The device command initiates a timing sequence as previously described. (Refer to section VI for device control format on the data lines.) At time slot 6, the transmit device set gate sets the transmit device enable flip-flop. The transmit device enable flip-flop will remain set until the end of time slot 4 of the following byte, which specifies which of the three device codes is to be utilized. (Refer to section VI for amplifying data byte definition.) The 1-0 state of the first 2 bits of the amplifying data byte, indicating a device 1 control character, permits the transmit device 1 flip-flop to set at time slot 4 of this cycle. The transmit command decoded output applied to input/output control no. 2 results in the generation of an indicator signal to the IOM. The indicator signal provides an acknowledgment to the IOM in response to a proper command sequence. The transmit data if high signal is active when the transmit word is received and is used for parity checking and detection. The signal is also used by input/output control no. 2 for generating a request signal to the IOM for the first data byte to be transmitted.

c. After a request is generated by input/output control no. 2, the IOM pulses the enable line. The occurrence of the enable signal and a transmit address byte sets the transmit enable latch and sends a transmit enable signal to input/output control no. 2. The transmit enable signal is used to generate a strobe pulse for IOM input data. At time slot 6 of this data transfer, the transmit enable flip-flop is set, and is reset at the end of time slot 5 of the next data transfer. The data transfer that follows the enable sequence is data to be transmitted by the modem. The transmit enable flip-flop signal allows the data to be stored in the transmit buffer at time slot 4, assuming no parity error or transmit timeout has been detected. The transmit enable flip-flop signal also resets the transmit enable latch. The circuit is now prepared for the next input data sequence. Upon the detection of a transfer timeout or parity error, the transmit buffer is inhibited and will transmit all zeros.

d. A parity check is performed on all data transferred from the IOM. Parity is checked at the beginning of time slot 3. If parity is incorrect, the parity detect gate will set the parity error latch and the latch will remain set until the EOB is detected from the IOM. When the parity error latch sets, the transmit buffer transmits zeros for the remainder of the message.

e. The input/output control no. 1 contains device stop and EOB circuits, which are logically implemented in the same manner. Therefore, only the device stop circuit will be described. The first data transfer in this sequence is identical with the transmit command described previously. The second data transfer consists of a control/command byte which contains either bits 0 and 7 or bits 0 and 6 active, signifying a device stop or an EOB. At time slot 6, upon detecting a device stop, all transmit and receive circuitry is reset and reflects a standby condition.

5-14. Input/Output Control No. 2 Detailed Description (fig. 5-21, FO-7). Input/output control no. 2 provides the dc interface required for communication with the IOM and also generates the indicator and transmit receive requests for the IOM. Refer to figure 5-22 for input/output control no. 2 timing.

a. When a transmit device 1 command is properly stored in input/output control no. 1, the transmit command decode signal sets the command acknowledge circuit. After the next clock pulse, the command acknowledge circuit is reset, producing an indicator pulse which is supplied to the IOM interface. The indicator pulse, a nominal 190-nanosecond signal, is used to acknowledge receipt of a command sequence. The indicator pulse is supplied to the transmit request generation circuit, along with a transfer data if high signal from input/output control no. 1, for generating a request to the IOM for transfer of data. The request, which is generated during the time the modulator is outputting a start pattern, is to ensure that data is ready and stored when the modulator requests the first data word. When the word (8-bit byte) is requested (strobed) by the modulator, the data strobe signal from the data formatter causes another request to be generated. A request is generated with each data strobe signal until a transmit EOB is recognized. The effect of the transmit EOB is to cause the modulator to cease requesting data. The transmit EOB signal also generates one more request signal to the IOM.

b. The receive request generation is similar to the transmit request generation except that the receive request is generated at the beginning of the data available pulse. The data available pulse is received from the data synchronizer (demodulator) when an 8-bit data group is ready to be sent to the IOM.

c. The transmit timeout circuit is used when a transmit request is generated but not serviced by the IOM before the next transmit request is generated. The

result of a transmit timeout condition is that any subsequent data byte will be transmitted as all zeros.

d. Three conditions cause a strobe pulse to be generated for the IOM input data. The first condition is a receipt of an enable from the IOM in response to a receive request. Second is a receipt of an enable from the IOM following a transmit EOB, and third is a receipt of an input to register (ITR) command from the IOM. Any of the above conditions (when active) are applied to a data byte counter preset gate. The data byte counter preset gate presets the data byte counter to state 8 which then continues to count to state 15 (terminal count). Upon reaching terminal count, the data strobe register allows data to be strobed into the IOM for three clock times. After terminal count, the data byte counter returns to state zero and counts to state 2, which resets the input/output control no. 1 transmit control flip-flop and ITR latch. The data byte counter then proceeds to state 4 and locks up.

e. Data, received by the demodulator in serial form, is stored in parallel in data storage. The data is stored by a data available signal and a receive request being generated. The receive request is used as the clock pulse for the data from the demodulator. The data from data storage is then transferred to data gating. Data gating provides the selection of either receive data bits or status bits, which is controlled by the presence or absence of the status byte signal. The status byte signal is active during an ITR command or a transmit EOB and transmit enable. (Refer to section VI for status byte bit definition.)

f. The output from data gating is used as an input to the parity generator as well as an input to the data line drivers. When the data strobe pulse occurs, the data and parity are simultaneously strobed to the IOM. The IOM senses a negative-going pulse (nominal 190 nanoseconds) as a logic one. The parity generator provides odd parity for the data transfer.

g. The demodulator will detect two EOB commands on each NATO and spare link format to accommodate multiple message lengths. The first EOB enables software to determine the proper message length; the second informs the modem to search for another synchronization pattern. When operating in either the TADIL-B or MBDL data links, every EOB is sensed and passed on to the demodulator. The receive EOB signal is passed through receive EOB detect gating with the resultant output used in the demodulator. When the input to the receive EOB flip-flip is active high (implying NATO or spare data link), the receive EOB detect gating is disabled by EOB control gating. When the first receive EOB signal is received, the receive EOB flip-flop is set at the trailing edge of the EOB signal. The second EOB is passed through the receive EOB detect gating to the demodulator. At the trailing edge of the EOB, the receive flip-flop is reset.

h. The inhibit data gate detects when power is turned on or off. The result of the detection initializes the logic to a standby condition and simultaneously inhibits the data line drivers. The preset signal defines a master reset condition or a power turnon preset. The device inhibit signal defines initial power turnon or power supply malfunction.

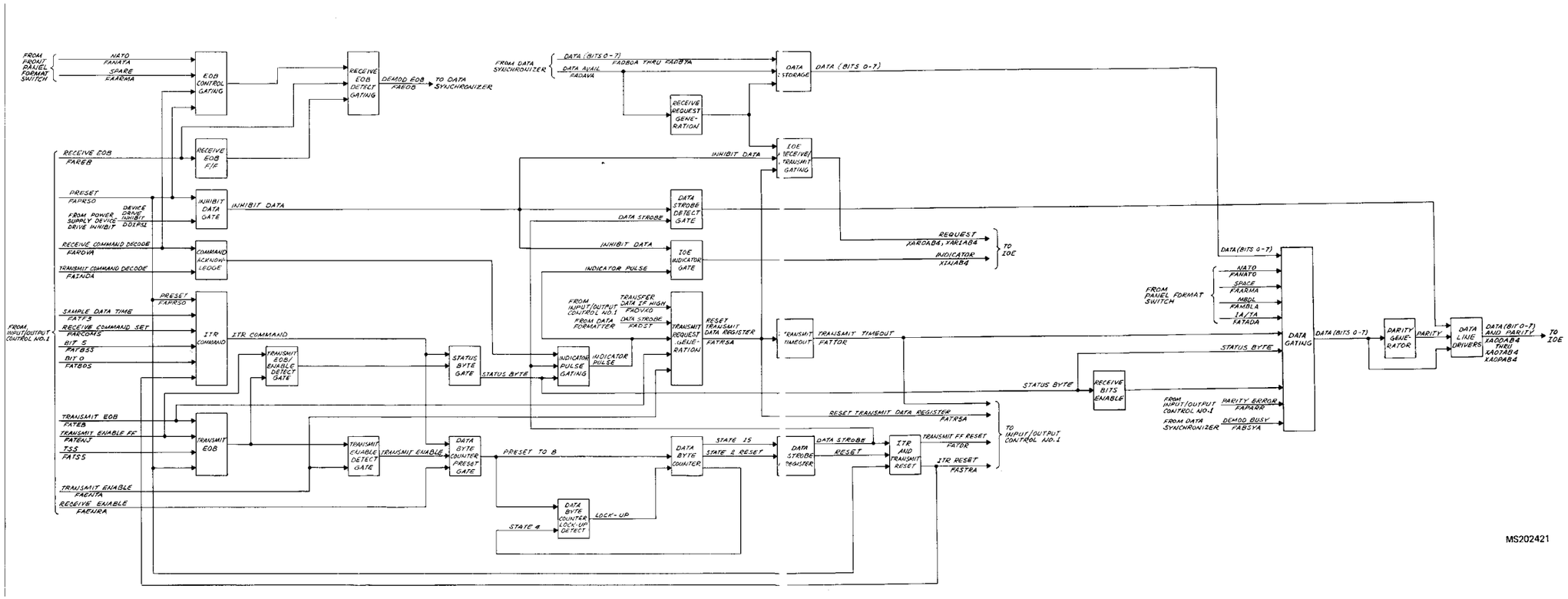


Figure 5-21. Input/Output Control No. 2 Block Diagram

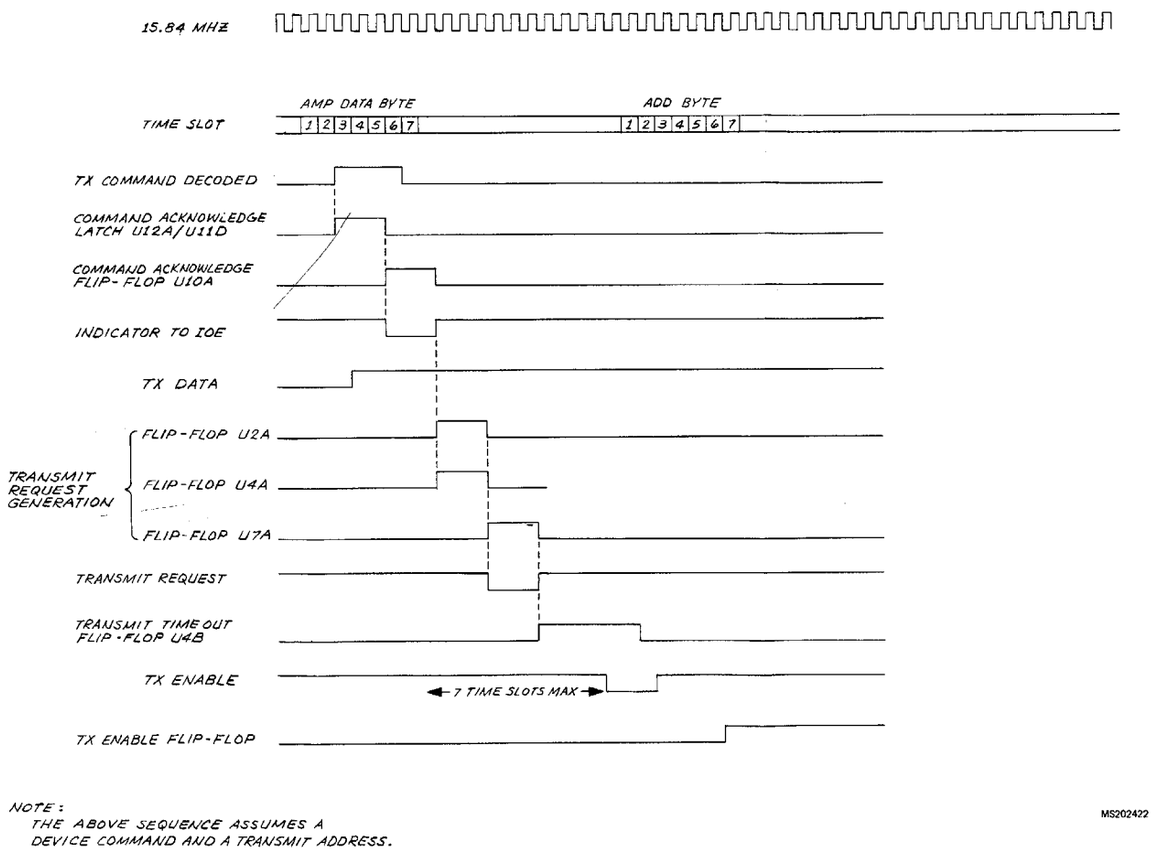


Figure 5-22. Typical Input/ Output Control No. 2 Timing

Section IV. IBL MODE CONTROL

5-15. IBDL Mode Control Detailed Description (fig. 5-23, FO-8). The interim battery data link (IBDL) mode control provides for battery data link information exchange if the automatic data processing equipment (ADPE) malfunctions. The IBDL mode will maintain the cross-tell of fire unit status among the batteries of the air defense system. The IBDL mode requires the use of a dedicated modem (modem no. 17) and all the modem analogs currently operating in the MBDL mode. Under normal conditions, data transfer between the battalion and the batteries and timing is under control of the ADPE. In the event of a computer failure, all batteries are interrogated by the IBDL time base. The IBDL mode may be selected by a switch on the data terminal system front panel if normal system power is used or, if there is failure of main power, the emergency power sensor automatically switches the data terminal system to the IBDL mode. Emergency backup power is also supplied to the ADPE CMOS memories.

a. Upon selection of the IBDL mode, a remote start (interrogation signal) is transmitted to all the batteries. Refer to figure 5-24 for IBDL normal cycle operation. The IBDL mode signal presets the remote start flip-flop and enables the IBDL timer. The IBDL mode signal also enables all modem analogs for transmission of the remote start signal. The IBDL timer, upon receiving a bit clock from the modem no. 17 demodulator, allows a negative remote start signal to be generated for 9 counts. The remote start signal is processed by the modem no. 17 modulator and sent to all modem analogs for transfer to the batteries.

b. The return messages from the batteries are selectively examined one channel at a time. When a fire unit is active, a channel in use signal is supplied to the scan counter enable gate, which allows the scan counter to search for an active channel. The scan counter uses a channel select decoder to synchronously pulse channels 1 thru 32 until an active channel is detected. Only active modems operating in the MBDL format are selected. When an active channel is detected, cycle control inhibits the scan counter from selecting another channel, and waits two complete cycles before continuing the search. The two cycles are required for interrogation and examination of each battery to allow two fire units to report battery data link messages. Information is processed by the active channel until an EOB occurs or the IBDL timer counts to 99. Since cycle control functions as a clocked set and reset latch, the cycle only occurs on alternating EOB or IBDL timer count 99. If no channels are active, the scan clock will allow the scan counter to continuously search for an active channel.

c. Each channel selected must respond to the remote start signal by transmitting a ready start signal within 55 bit periods. The ready start signal, after demodulation processing, is received at the IBDL start detect gate as a negative IBDL start pulse. The IBDL start detect gate requires four conditions, as follows, to justify a valid start:

(1) Bit clocks occurring.
(2) Completed remote start transmission.
(3) IBDL start received.
(4) No timeout detected.

If the above conditions are present, a start pulse of one bit time is generated. The start pulse causes all timing to resynchronize and start at zero. The start pulse also sets the valid start flip-flop, which initiates a transmit enable to the modem no. 17 modulator. The transmit enable signal allows a ready start pattern to be sent back to the fire unit prior to data transmission.

d. If the ready start signal is not received before bit time 55, as shown in figure 5-25, data transmission is inhibited and the IBDL timer will count to 99 and resequence.

e. The EOB is a one bit time pulse occurring at either bit time 60 or 98, depending upon whether the operating mode is normal or abnormal, respectively. The EOB signal is sent to the modem no. 17 demodulator to reset the start-of-message detector and look for another start.

f. At the end of data transmission, the IBDL logic again transmits a remote signal to all batteries and the sequence is repeated.

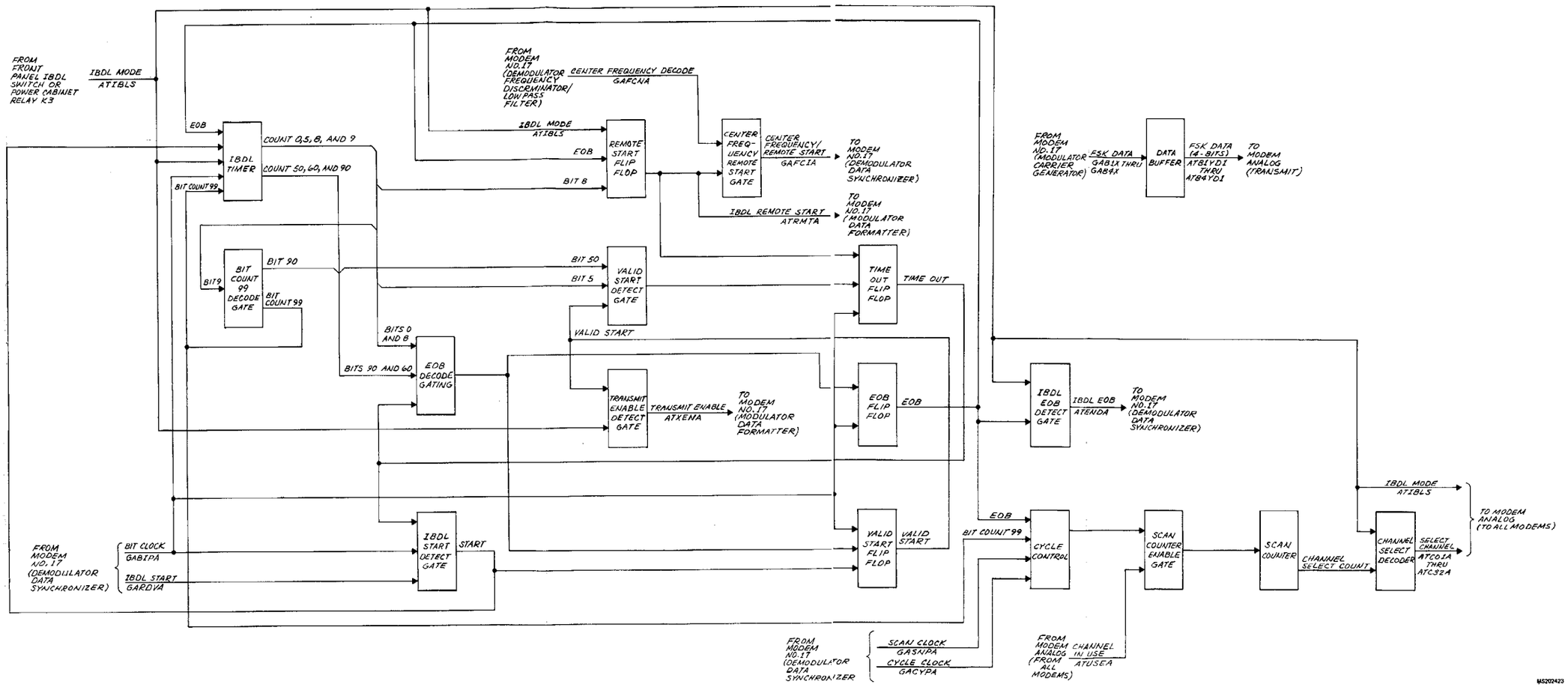


Figure 5-23. IBDL Mode Control Circuit Block Diagram

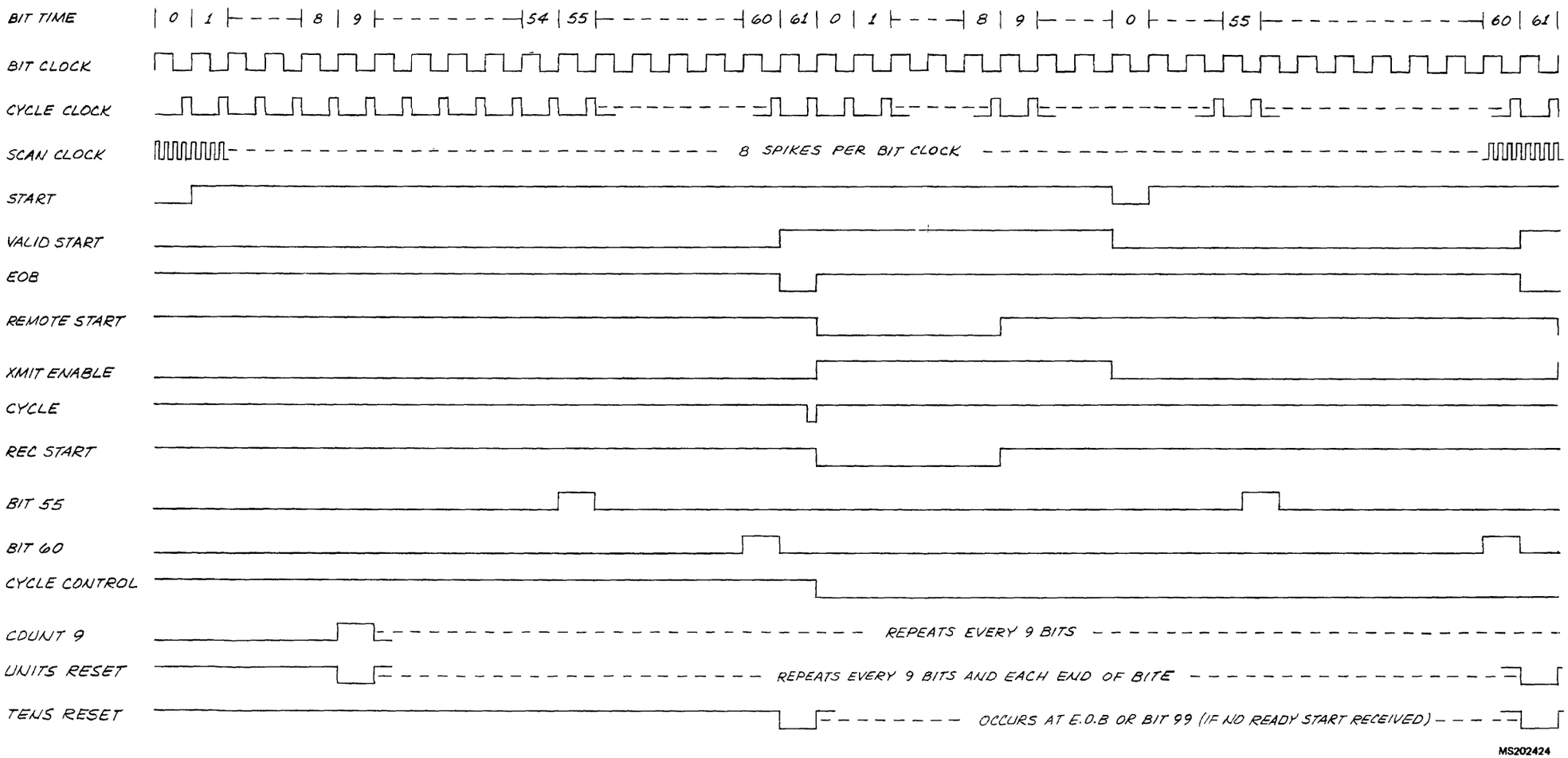


Figure 5-24. IBDL Normal Cycle Operation Timing Diagram

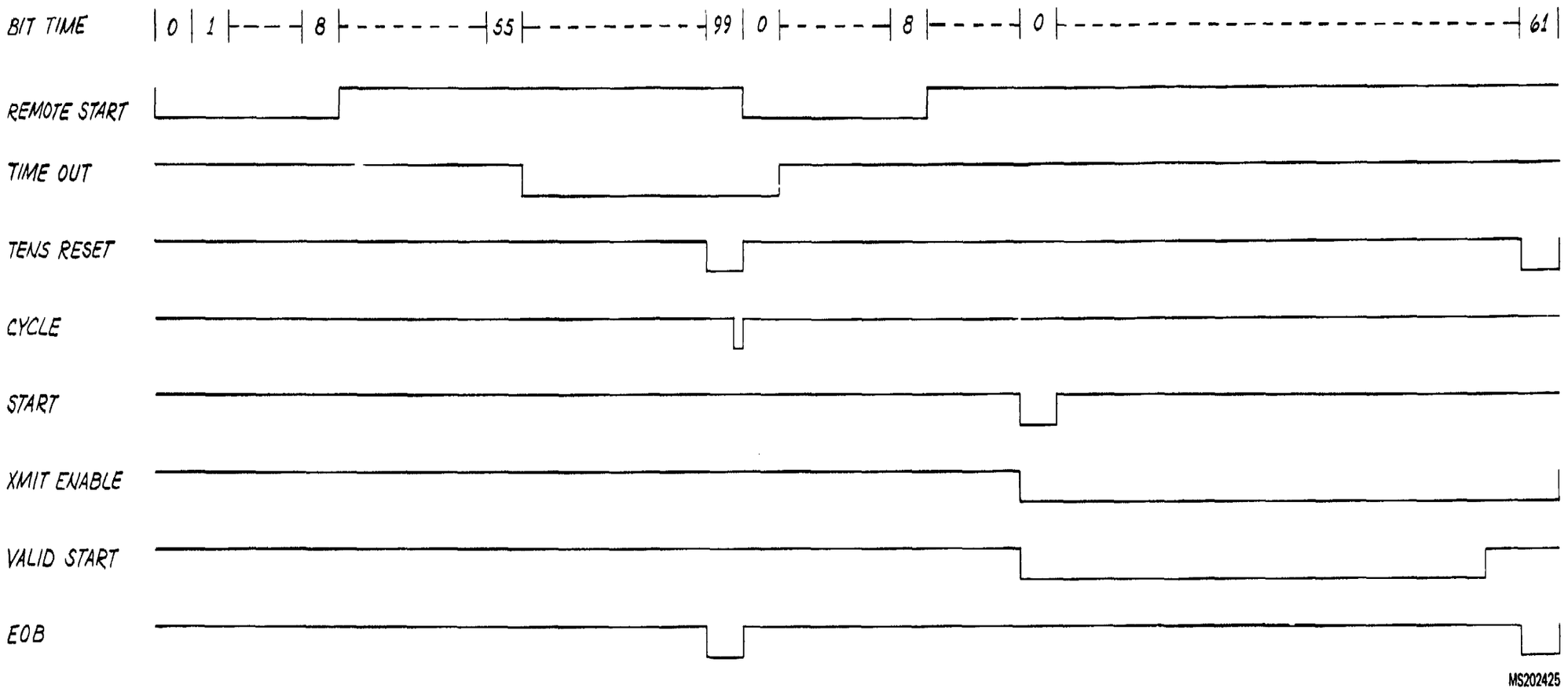


Figure 5-25. IBDL Abnormal Cycle Operation Timing Diagram

Section V. COMMON TIMING

5-16. Common Timing Detailed Description (fig. 5-26, FO-9). Common timing contains a 15.84 MHz oscillator generator, buffers, frequency dividers, and clock drivers required to provide four timing lines common to all modems. Common timing also contains a fault detection circuit which detects the absence of any of or all the four basic timing lines. Refer to figure 5-27 for common timing circuit clock timing.

a. The base clock is generated by a 15.84-MHz oven-controlled oscillator which ensures an accuracy rate of better than one part per million. The 15.84-MHz base time was selected for compatibility with the input/output computer rate of 16 MHz. The base time is divided by 10 and three to obtain a 1.584-MHz clock and 5.28-MHz clock respectively. The 5.28-MHz clock is not used. The 1.584-MHz clock is used for synchronization and carrier generation. The 1.584-MHz clock time is divided by 33, using divide by 11 and 3 frequency dividers, to obtain a 48-kHz clock. The 48-kHz clock is required for bit rate generation and synchronization. All four timing lines are then used to provide the time base from which all other timing signals are derived and used within the modem.

b. Clock drivers are provided to eliminate excessive clock distortion and to accommodate high fan-out requirements.

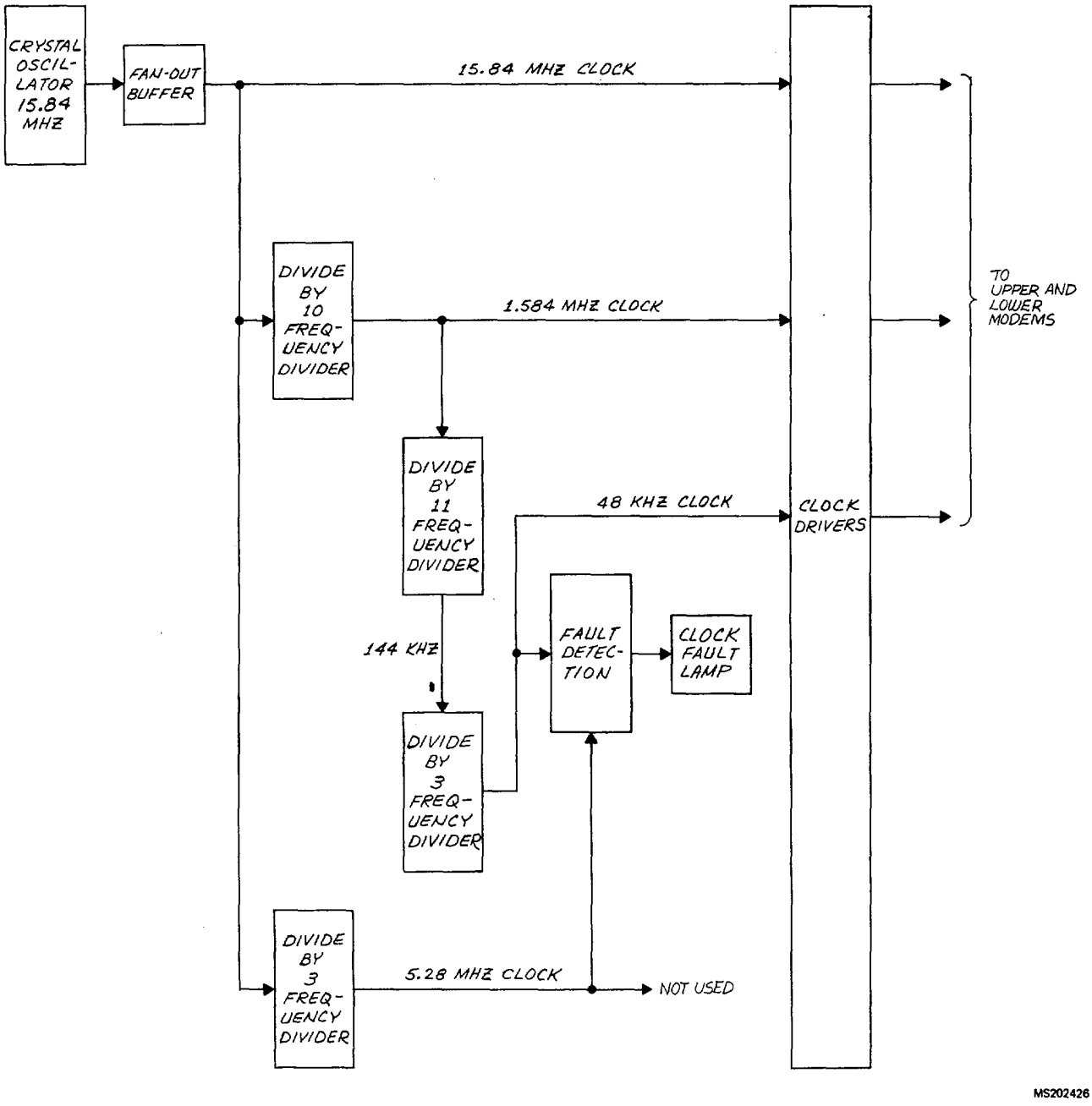


Figure 5-26. Data Communications Timing Block Diagram

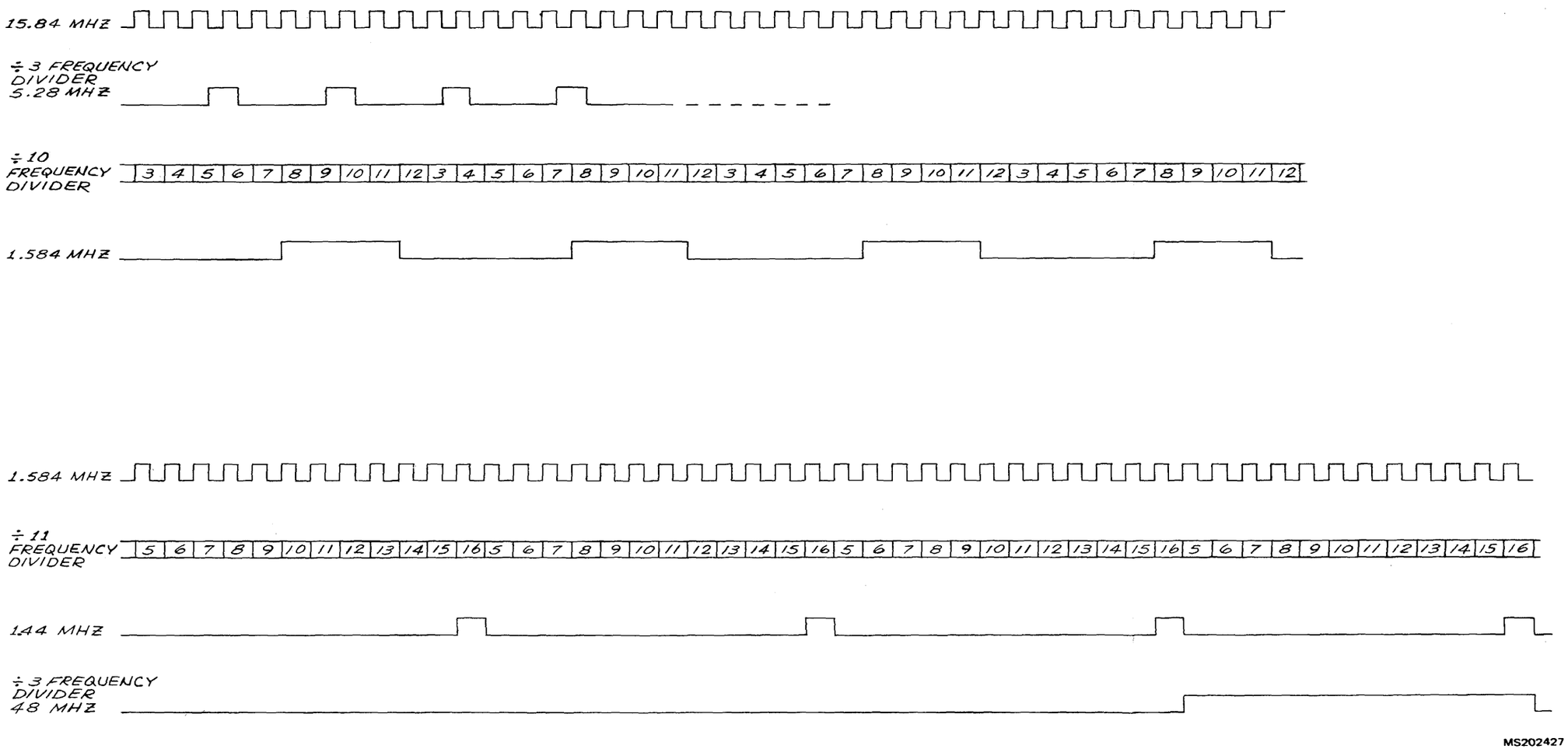


Figure 5-27. Data Communications Timing Circuits Clock Timing Diagram.

Section VI. EXTERNAL SUBSCRIBER PATCH AND IOM INTERFACE

5-17. External Subscriber Patch Interface (FO-10). The external subscriber patch interface provides patching, line-only monitoring, equipment-only monitoring, or monitoring without interruption of data communication signals. The interface also provides test capabilities and diagnostic connections used in conjunction with fault isolation procedures. The external subscriber patch interface consists of a communications patching panel and demarcation panel. The communications patching panel provides the patching and monitoring capabilities and contains eight sets of jacks for each modem. The demarcation panel provides the common access for all data communication interfaces to external shelter and remote subscribers. All interconnections are applied through rfi filters, which provide emi suppression and surge protection against lightning-induced transients.

5-18. IOM Interface (fig. 5-28, FO-11). All transfer of information (commands or data) between the IOM and a modem is performed using a total of 14 lines. The 14 lines consist of nine information lines (eight information bits plus parity), a command line, an enable line, an indicator line and two request lines. The IOM contains eight IOEs which interface each with four modems. Specific commands detected by a modem from the IOM are device (DEV), input to register (ITR), device stop (DS), end of block (EOB), and master reset (MR). Refer to table 5-11 for a description of the various commands required to control a modem. All commands are specifically addressed to a particular modem except for master reset, which is used by all modems conditionally. Addressing a modem for a command sequence is performed by one of the two information lines assigned to each modem. Even numbered bit positions (bits 0, 2, 4 and 6) of the information lines are assigned to the demodulation, and all odd bit positions (bits 1, 3, 5 and 7) are assigned to the modulator.

a. When power is first applied to a modem, the modem is in a standby (idle) mode ready to respond to commands received from the IOE. A normal command sequence from the IOE is an ITR followed by two DEVs. The ITR command requires two bytes. The first byte is the address/command, defined by the simultaneous presence of a pulse on one of the eight information lines (0, 2, 4 or 6 receive address) and the command line. The first byte allows the second byte to be accepted only by the modem addressed. The second byte is an ITR command which is recognized by the simultaneous presence of pulses on bits 0 and 5 of the information lines. Refer to table 5-12 for control format information line function definition. In response to the second byte, the modem inputs a status byte to the IOE defining which type of link (message format) is selected by the modem. The definition of the bits in the status byte is as follows: Bit O--Demodulator busy (receive mode)

Bit 1-Transfer parity error
Bit 2*-Transmit request time out
Bit 3-Spare format
Bit 4-MBDL format
Bit 5-IA/TB format
Bit 6-NATO format
Bit 7-Not used
Bit 8-Parity (odd)
*Transmit request time out is defined as a modem not being serviced between any two consecutive transmit request pulses.

Simultaneously with the status byte, the indicator line is pulsed by the modem indicating acknowledgment of a command sequence.

b. The second command received by a modem is a DEV. The DEV command sequence requires three bytes. The first byte is (address/command) as previously described for the ITR; the second byte defines the DEV command as shown in table 5-13. The third byte, if a DEV 1, activates the demodulator and allows reception of incoming data when a synchronization pattern is detected. The last command to initialize a modem is also a DEV command except the modulator address (bit 1, 3, 5 or 7 transmit address) is used in the first byte of the command sequence and the third byte is either a DEV 1, DEV 2, or DEV 3. Depending on the message format selected and whether DEV 1, 2 or 3 had been received by the modem, the modulator begins to output a start pattern. The start pattern for DEV 1, 2 or 3 is as follows:

(1) DEVI. For MBDL, the modulator transmits the remote start and ready start preceding the data.

(2) DEV 2. Transmits synchronization pattern (ready start for MBDL) preceding the data.

(3) DEV3. Initiates loop test (output of modulator is fed back to input of demodulator) and reverts to normal operation upon receipt of the EOB for the modulators.

In the above two command sequences, the indicator line is pulsed to the IOE for each command received.

c. Upon receipt of the third byte of the modulator command sequence, a transmit request pulse is generated by the modem, requesting the first data byte to be transmitted. In a manner similar to the addressing of the modems by the IOE, is eight request lines to the IOE with corresponding bit positions for a particular modem. As an example, if bits 0 and 1 are used by the IOE to address a demodulator and modulator respectively, the modem will use request lines 0 and 1 to signify request for service from the same demodulator and modulator. The servicing

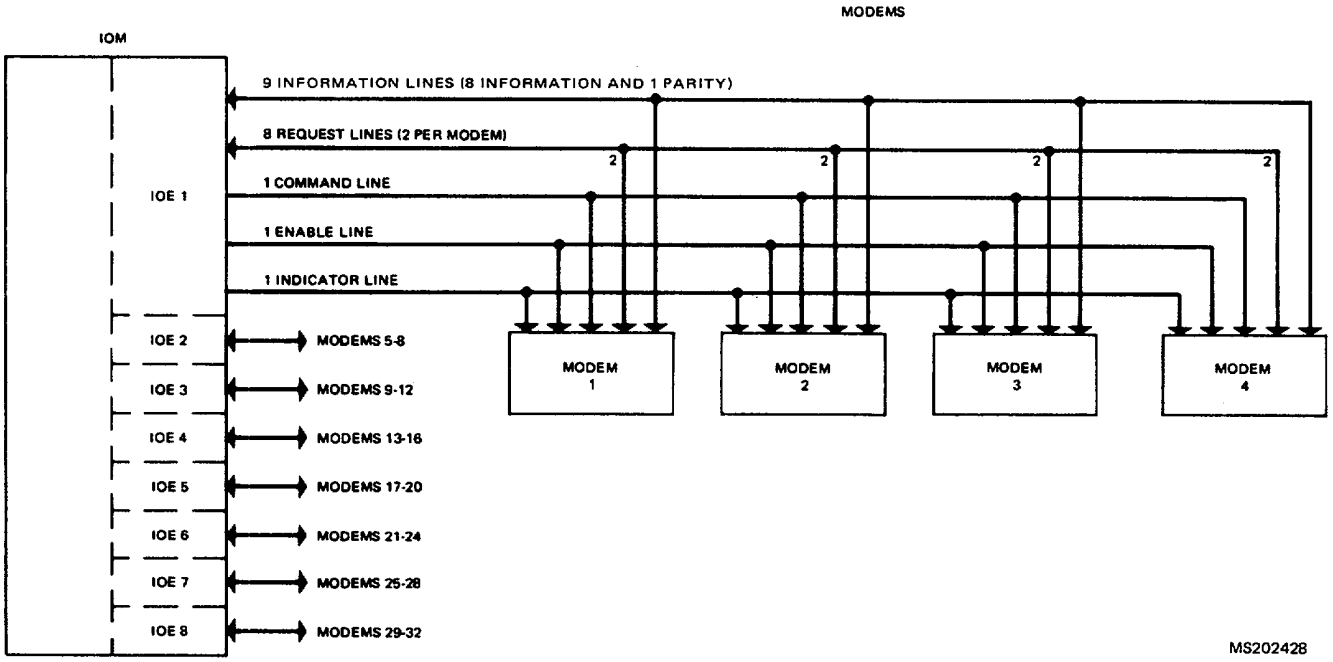


Figure 5-28. Modem-to-IOM Interface Block Diagram

of the first transmit request generated to the IOE is determined by the modem detecting a simultaneous pulse on the modulator address and enable line from the IOE. This byte informs the modem that the next byte on the information lines is to be accepted as data to be transmitted. The modem transmits data until the detection of an EOB command. The EOB command is detected in the same way as an ITR command except that bits 0 and 6 are used in the second byte. The EOB command returns the modulator to an idle state. In addition, when an EOB is detected for the modulator, the modem inputs a status byte to the IOE and simultaneously pulses the indicator line.

d. When the demodulator recognizes a start pattern, a receive request is generated to the IOE. At the end of the receive request, the IOE sends an EOB command to the demodulator. The demodulator EOB command differs from the modulator in that the modem performs no interrupt and status posting, and does not return to an idle state. The demodulator after receiving an EOB command remains active and immediately begins to search for a new start pattern.

e. A device stop command is detected by bits 0 and 7 in the second byte, indicating a malfunction. The device stop command either resets the modulator or demodulator (whichever is addressed) and waits for a DEV command to be initiated.

Table 5-11. Command/Control Sequence

Definition	TADIL-B/Intra Army MOD (XMIT)	DEMOD (RCV)	Spare MOD (XMIT)	DEMOD (RCV)	NATO MOD (XMIT)	DEMOD (RCV)	(MBDL) Missile battery D.L. MOD (XMIT)	DEMOD (RCV)
1 Master Reset, do not talk to Computer, provide IDLE to MOD (Modulator).	MR	MR	MR	MR	MR	MR	MR	MR
2 For DEMOD, a command to prepare to receive after MR or power turn-on. Transfer data upon sync detection For MBDL Modulator, it means send Remote Start and Ready Start followed by data until EOB is sensed.	-	DEV-1	-	DEV-1	-	-DEV-1	DEV-1	DEV-1
3 Send sync pattern (Ready Start for MBDL) and commence requests for data until EOB.	DEV-2	-	DEV-2	-	DEV-2	-	DEV-2	-
4 Loop test, connect MOD to DEMOD, send sync (ready start) pattern, and request data until EOB which resets DEV-3.	DEV-3	-	DEV-3	-	DEV-3	-	DEV-3	-
5 Device stop, go to MR condition.	DS	DS	DS	DS	DS	DS	DS	DS

Table 5-11. Command/Control Sequence-Continued

Definition	TADIL-B/Intra Army MOD (XMIT)	DEMOD (RCV)	Spare MOD (XMIT)	DEMOD (RCV)	NATO MOD (XMIT)	DEMOD (RCV)	(MBDL) Missile battery D.L. MOD (XMIT)	DEMOD (RCV)
6 End of Block, cease communications with computer until DEMOD detects new sync or MOD receives a DEV command, demodulators look for sync, modulators revert to IDLE condition and commence interrupt sequence reporting status consisting of demodulator, Time Out, and Transfer Parity error, channel type.	EOB	EOB	EOB	EOB	EOB	EOB	EOB	EOB
7 Generate interrupt sequence and post status.	I	I	I	I				
8 Provide status, even if in the MR or DS condition.	ITR	ITR	ITR	ITR	ITR	ITR	ITR	ITR

Table 5-12. Device Control Format on Information Lines

Bits present during control phase									Function
Parity	B7	B6	B5	B4	B3	B2	B1	B0	
1	0	0	0	0	1	0	0	1	Device Command (DEV)
1	0	1	0	0	0	0	0	1	End-of-Block (EOB)
1	1	0	0	0	0	0	0	1	Device Stop
1	0	0	1	0	0	0	0	1	Input to Register (ITR)

Table 5-13. Amplifying DEV Control Character

Parity	B7 (LSB)	B_6	B_5	B_4	B_3	B_3	B_1	B_0 (MB)	
DEV 1	1	0	0	1	0	0	0	1	0
DEV 2	1	0	0	1	0	0	1	0	0
DEV 3	0	0	0	1	0	0	1	1	0

Section VII. POWER DISRTIBUTION

5-19. Data Communications Power Distribution (FO-12). The data communications power distribution consists of primary power, low voltage distribution, and power fault monitoring.

a. *Primary Power*. Primary power for data communication circuits is provided by the system power cabinet. Primary power includes complementary + 135v and -135v referenced to dc center tap (common). Primary power consists of normal and emergency power; refer to TM 9-1430-655-20-8 for a schematic diagram of the power cabinet normal and emergency power circuits.

(1) Normal +135v and -135v power is applied to both upper and lower modem dc/dc converters 1A1A2A5PS1 through 1A1A2A5PS4 and 1A1A2A7PS1 through 1A1A2A7PS4 from the power cabinet DATA COMM circuit breaker. Local turnon and turnoff for each dc/dc converter are provided by ON-OFF switches located on the data communications control panel.

(2) Emergency + 135v and -135v power is applied only to 1A1A2A7PS1 in the lower modem. During an emergency condition, when primary power is lost, battery power is supplied to 1A1A2A7PS1 from the system power cabinet. This dc/dc converter supplies emergency power for the IBDL and clock circuits to sustain IBDL operation and to the ADPE for data retention in the CMOS memories. IBDL operation is automatically initiated by a power failure (refer to paragraph 5-15).

b. Low-Voltage Distribution. Low voltage is provided from identical dc/dc converters. Each dc/dc converter provides + 15v, +5v, and -15v low voltage power for the data communications circuits. Within the upper and lower modems, each dc/dc converter provides power for groups of four modems. This distribution provides a convenient fault isolation method for determining power failure when a specific group of four modems fails at the same time.

(1) Power turnon for each modem is controlled by a POWER switch located on the control card of that modem. For example, POWER switch S3 on modem control card A1102 provides +5v (+5PSIA) to cards A1103 through Al 109 which make up modem no. 1. In addition, + 15v and - 15v are applied directly from the dc/dc converter to provide the necessary power for modem operation.

(2) Low-voltage power for circuits contained in the data communications card cage is provided via the lower modem from dc/dc converter 1A1A2A7PSI. This dc/dc converter is the emergency power supply; therefore, the data communications card cage cards which are part of the IBDL circuit have constant power applied.

(3) During IBDL operation, +5v (+5PS5A/B), +15v (+ 15PS5A/B), and -15v (- 15PS5A/B) low voltage power is supplied by the emergency power supply 1A1A2A7PSI in the lower modem. When the IBDL mode is activated, only the IBDL portion of each modem is activated, and power consumption is reduced to accommodate the single emergency power source. The + 5v output of the emergency power supply is applied to cards A 101 and A1301 in both the upper and lower modems. This voltage provides normal and emergency power to sustain IBDL and clock operation and to the ADPE for data retention in the CMOS memories. A1 101 provides pull-up signals +5PUPI through +5PUP4; A1301 provides +5v pull-up for clock signals AT5M2D4, ATIS5MD4, AT48KD4, and AMIM5D4.

c. Power Fault Monitoring. If a dc/dc converter fails, internal control logic shuts down that unit and consequently inhibits the associated modems while producing fault indications on the data communications control panel and on the INT fault lamp on the dc/dc converter.

(1) Power status of each dc/dc converter is monitored on the ON-FAULT indicators located on the data communication control panel. With primary power applied, each dc/dc converter is turned on by the respective ON-OFF switch. For example, upper power supply no. 1 (1A1A2A5PS1) is turned on by ON-OFF switch S4 on the data communications control panel. This applies a dc common signal (PS1CTL) to logic control circuits in the dc/dc converter, turning on internal low-voltage power supplies. Auxiliary +5v (+5AUX1) power produced in the logic control circuits lights the ON portion of the ON-FAULT indicator. With power applied, a device drive inhibit signal (DDIPSI) from the dc/dc converter is applied to associated modems for use as power fault logic. When the dc/dc converter fails, logic control circuits shut down power and apply a fault signal (PS1 FLT) to light the FAULT portion of the ON-FAULT indicator; the ON indicator goes out when power fails.

(2) LAMP TEST S10 on the data communications control panel permits testing of all front-panel lamps and the INT and EXT fault lamps on the dc/dc converters. Except for lamp testing, the EXT fault lamp is inactive in the data communications power circuits.

Section VIII. CABLING AND FRONT PANEL SCHEMATIC DIAGRAMS

5-20. Cabling Diagram (FO-13). A cabling diagram identifies all elements of the equipment and shows how they are electrically related. Included on the diagram are reference designators, part numbers, drawing (wire list) numbers, and references to wiring diagrams.

5-21. Front Panel Schematic (FO-14). A data communications control panel schematic diagram identifies controls and indicators and their electrical details, illustrates pin arrangements, and identifies signal mnemonics associated with a particular control function.

Section IX. GLOSSARY OF TERMS

5-22. General. This glossary provides a convenient reference to the terms used in the data communications theory. No attempt is made to define standard electronic terms used in this manual. Terms that may vary in context (bit, message, etc.) and terms peculiar to data communications (idle mode, bit clock, etc.) are included. Terms that are sufficiently described in the text (data formatter, zero crossing window, etc.) are also omitted.

Address	The selection of a modem for a command sequence using two information lines assigned to each modem. The address is used in conjunction with the enable or command lines.
Advance/retard data synchronization	A method of detecting early, late, or on-time data transitions and advancing or retarding timing until proper synchronization is obtained.
Center frequency	A carrier frequency which is used as a base reference between a transmitting and a receiving device and is modulated to carry usable information.
Check group	Parity bits for data groups which ensure that the transfer between the computer and the modem is free of errors.
Command line (from IOM)	A line used in conjunction with the information lines to perform address selection, and to signify a command operation during the transfer of information. The line is also used in conjunction with the enable line to signify a master reset.
Data byte	An 8-bit data group, accompanied by a parity bit, which is transferred over nine information lines.
Data mode	The last mode of operation following idle, remote start, and ready start modes, which allows the transfer of data until the detection of an EOB.
Data strobe	A signal, in the data mode, which allows data to be transmitted or received at the correct time sequence selected by the FORMAT and BPS switches.
Device (DEV)	Three commands which are used by the computer to enable the modems.
Device stop (DS)	Identifies a malfunction and places the modems in a master reset condition. Modulator transmits idle pattern, and demodulator is not searching for sync pattern.
Differential frequency shift keying (DFSK)	A method of encoding a carrier frequency shift frequency so that a change in the modulation frequency between two contiguous time slots represents a logic one, whereas no change represents a logic zero. For NATO format, which utilizes DFSK, the initial bit of each message is encoded as high frequency (i.e., a logic one).
Enable line (from IOM)	A line used in conjunction with the information lines to perform address selection and signifies transfer of information to or from the IOM. The line is also used in conjunction with the command line to signify a master reset.
End of block (EOB)	Denotes an end of message and allows the modulators to interrupt and post status. The demodulator uses two EOBs. One determines message length, and the other starts a search for another synchronization pattern.
Frequency shift keying (FSK)	A method of encoding a carrier frequency so that the lower and higher modulated frequencies for specific time slots are mark and space frequencies, respectively.
Idle mode	Defines a condition when the computer is not providing information to the modem.
Indicator line (to IOM)	A line used to acknowledge receipt of a special command and to initiate a device interrupt.
Information lines	Nine lines used for transmitting information between modems and the IOM. The nine lines consist of eight bits of data and a parity bit.
Input to register (ITR)	A sequence used by the computer to determine the status of a modem. The modem responds by sending an 8-bit status byte.
Interrupt	A sequence used for acknowledge, and to signal the computer that an error has occurred.

Loop test (DTS)	Software-generated test by which the modulator is connected to the demodulator and a synchronization pattern is generated and detected. The test message is looped back to the ADPE for comparison.
Marker bit	The bit occurs at the beginning of each data byte and indicates that data is available. The bit is modem-generated for the IA/TADIL-B format and computer-generated for all other formats.
Mark frequency	The lower frequency which reflects a logic one.
Master reset (MR)	A sequence which is evidenced by pulses on both the command and enable lines, resetting the modem to the idle mode. The master reset is also used when power is turned on.
Parity	An additional bit to an eight-bit byte that causes the nine bits to reflect an odd number of ones.
Ready start mode	A synchronization pattern which starts each message frame to ensure that the timing of the sending station is the same as that of the receiving station.
Receive request	Supplied to the IOM when an 8-bit data byte is ready to be transferred from the modem.
Remote start mode	An interrogation signal generated for the MBDL format only and sent to external subscribers at the beginning of each transmission cycle.
Request lines (to IOM)	Two lines used for each modem which reflect receive or transmit requests, and which correspond to the modem address selected.
Transmit request	Supplied to the IOM when the modulator is ready to receive an 8-bit data byte from the IOM. Space frequency The higher frequency which reflects a logic zero.
Status byte	An 8-bit byte which reflects the message format selected, parity, transfer parity error condition, transmit request time and condition, and whether the demodulator is busy.

*Us. GOVERNMENT PRINTING OFFICE: 1996 - 733-072/40050

By Order of the Secretary of the Army:

E. C. MEYER
General, United States Army
Chief of Staff

Official:

ROBERT M. JOYCE
Major General, United States Army
The Adjutant General

Distribution:
To be distributed in accordance with DA Form 12-32, Organizational Maintenance requirements for the AN/TSQ-73 Air Defense Guided Missile System.

*US GOVERNMENT PRIN'ING OFFICE 1984--746-036/3453 Region #4

TEAR ALONG PERFORATED LINE

RECOMMENDED CHANGES TO EQUIPMENT TECHNICAL PUBLICATIONS

SOMETHING WRONG WITH THIS PUBLICATION?

FROM: (PRINT YOUR UNIT'S COMPLETE ADDRESS)

DATE SENT

PUBLICATION NUMBER	PUBLICATION DATE	PUBLICATION TITLE

BE EXACT. . .PIN-POINT WHERE IT IS

PAGE NO.	PARA-GRAPH	FIGURE NO.	TABLE NO.

IN THIS SPACE TELL WHAT IS WRONG AND WHAT SHOULD BE DONE ABOUT IT:

PRINTED NAME, GRADE OR TITLE, AND TELEPHONE NUMBER

SIGN HERE:

DA FORM 1 JUL 79 2028-2

PREVIOUS EDITIONS ARE OBSOLETE.

P.S.—IF YOUR OUTFIT WANTS TO KNOW ABOUT YOUR RECOMMENDATION MAKE A CARBON COPY OF THIS AND GIVE IT TO YOUR HEADQUARTERS.

THE METRIC SYSTEM AND EQUIVALENTS

'NEAR MEASURE

. Centimeter = 10 Millimeters = 0.01 Meters = 0.3937 Inches
1 Meter = 100 Centimeters = 1000 Millimeters = 39.37 Inches
1 Kilometer = 1000 Meters = 0.621 Miles

'VEIGHTS

Gram = 0.001 Kilograms = 1000 Milligrams = 0.035 Ounces
1 Kilogram = 1000 Grams = 2.2 lb.
1 Metric Ton = 1000 Kilograms = 1 Megagram = 1.1 Short Tons

LIQUID MEASURE

1 Milliliter = 0.001 Liters = 0.0338 Fluid Ounces
1 Liter = 1000 Milliliters = 33.82 Fluid Ounces

SQUARE MEASURE

1 Sq. Centimeter = 100 Sq. Millimeters = 0.155 Sq. Inches
1 Sq. Meter = 10,000 Sq. Centimeters = 10.76 Sq. Feet
1 Sq. Kilometer = 1,000,000 Sq. Meters = 0.386 Sq. Miles

CUBIC MEASURE

1 Cu. Centimeter = 1000 Cu. Millimeters = 0.06 Cu. Inches
1 Cu. Meter = 1,000,000 Cu. Centimeters = 35.31 Cu. Feet

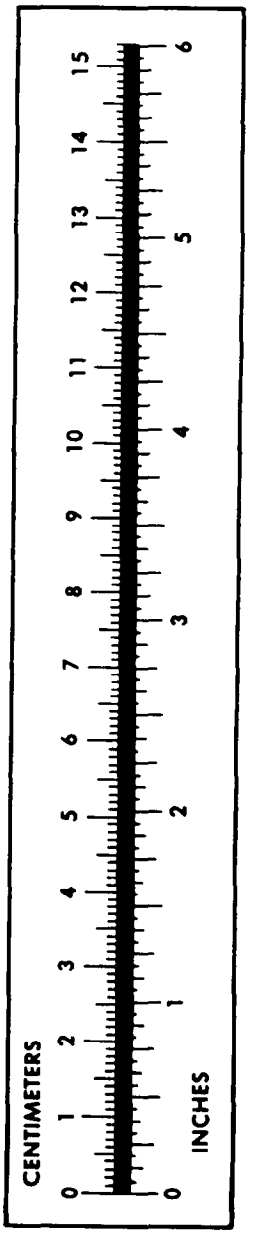
TEMPERATURE

5/9(°F - 32) = °C
212° Fahrenheit is evuivalent to 100° Celsius
90° Fahrenheit is equivalent to 32.2° Celsius
32° Fahrenheit is equivalent to 0° Celsius
9/5C° + 32 =°F

APPROXIMATE CONVERSION FACTORS

TO CHANGE	TO	MULTIPLY BY
Inches	Centimeters	2.540
Feet	Meters	0.305
Yards	Meters	0.914
Miles	Kilometers	1.609
Square Inches	Square Centimeters	6.451
Square Feet	Square Meters	0.093
Square Yards	Square Meters	0.836
Square Miles	Square Kilometers	2.590
Acres	Square Hectometers	0.405
Cubic Feet	Cubic Meters	0.028
Cubic Yards	Cubic Meters	0.765
Fluid Ounces	Milliliters	29.573
ıts	Liters	0.473
arts	Liters	0.946
allons	Liters	3.785
Ounces	Grams	28.349
Pounds	Kilograms	0.454
Short Tons	Metric Tons	0.907
Pound-Feet	Newton-Meters	1.356
Pounds per Square Inch	Kilopascals	6.895
Miles per Gallon	Kilometers per Liter	0.425
Miles per Hour	Kilometers per Hour	1.609

TO CHANGE	TO	MULTIPLY BY
Centimeters	Inches	0.394
Meters	Feet	3.280
Meters	Yards	1.094
Kilometers	Miles	0.621
Square Centimeters	Square Inches	0.155
Square Meters	Square Feet	10.764
Square Meters	Square Yards	1.196
Square Kilometers	Square Miles	0.386
Square Hectometers	Acres	2.471
Cubic Meters	Cubic Feet	35.315
Cubic Meters	Cubic Yards	1.308
Milliliters	Fluid Ounces	0.034
Liters	Pints	2.113
Liters	Quarts	1.057
ers	Gallons	0.264
ms	Ounces	0.035
ograms	Pounds	2.205
Metric Tons	Short Tons	1.102
Newton-Meters	Pounds-Feet	0.738
Kilopascals	Pounds per Square Inch	0.145
lometers per Liter	Miles per Gallon	2.354
meters per Hour	Miles per Hour	0.621



PIN: 051965-002